IET Power Electronics

Research Article

High step-up SVMC-based DC/DC converter for offshore wind farms

Received on 5th September 2018
Revised 15th December 2018
Accepted on 8th February 2019
doi: 10.1049/iet-pel.2018.5899

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Abstract: This study presents a high step-up scalable voltage multiple cell (SVMC)-based DC/DC converters, which have the features of high gain, low and adjustable components stresses and automatic input-current sharing in each input phase. In virtue of the above features, the converter is applicable for the DC collection grids for offshore wind farms. In this study, the converter in terms of working principle and property characteristics are analysed with four input phases and three SVMCs. The converter has also been evaluated in terms of the component stress and voltage conversion ratio against some other converters for high-power occasions. Moreover, a 2.5 MW simulation model and a 1.2 kW prototype were constructed for verification.

1 Introduction

Currently, offshore wind power generation becomes a promising region in wind power development with the advantage of the strong wind, stable wind speed and no occupation of land [1]. As for offshore wind farms with nearly offshore distance, high-voltage alternating current (HVAC) transmission technology is simple in structure and low in construction cost. However, with the increasing of the distance from the offshore wind farms to the land, HVAC transmission system has the problem of poor stability due to the grounding capacitor of cables [2–4]. High-voltage direct current (HVDC) transmission system becomes a popular choice when the offshore distance of the wind power generation station is longer than 50–130 km [5–7]. Traditional HVDC transmission technology based on line commutated converter has the problem of high cost of construction and maintenance due to the use of a large number of 50/60 Hz transformers [8–10]. In this regard, the HVDC transmission technology based on medium-voltage DC (MVDC) bus without bulky transformers has obtained much attention, which is shown in Fig. 1 [11–13]. However, there is no engineering example using this scheme today due to the solutions of the low-voltage (LV)–MV DC converter and the MV–HV DC converter are not mature. In general, wind turbine generator is rectified to 1–5 kV, while the output voltage of MVDC bus is usually 30–50 kV [11, 14, 15]. Therefore, the LV–MV DC converter should have the ability of high step-up conversion ratio. In the demand of photovoltaic and fuel cell power generation systems, some high step-up DC/DC converters such as cascaded converters [16, 17], coupled inductor converters [18, 19], switched capacitor converters [20–22], diode capacitor converters [23, 24] and some hybrid types

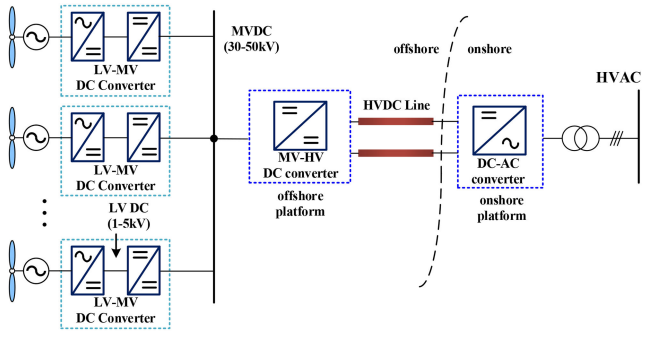


Fig. 1 *HVDC transmission technology based on the MVDC system*

[25–27] have gained much research results in recent years, However, these converters are mainly used in medium or small power level, which is difficult to be used as LV–MV DC converters because of their small capacity (voltage stress and current stress on components are too large to select or design).

Papers [11, 28–30] proposed a variety of topologies for LV–MV DC conversion. Two resonant capacitor DC/DC converters are proposed in papers [11, 28]. The converter proposed in [11] has the advantages of modularised structure, small resonant inductance parameters, low components voltage stress and easy to achieve soft switching. However, it needs a lot of capacitors and the power density of the converter is low. Meanwhile, the loss of passive devices in this converter is also high. Compared to paper [11], the number of components required by the converter proposed in paper [28] is effectively reduced; meanwhile, it also can achieve high-voltage conversion gain, but its voltage conversion ratio is exponentially increased, which is difficult to adjust smoothly. In addition, the resonant capacitor DC/DC converters usually have the problem of high-current stress on components. Paper [29] proposed a converter combined with a modular multilevel converter technology and a traditional boost converter, which has the advantages of high-voltage gain, modular structure and high reliability, but the current stress on the components is high, and the control strategy is relatively complex. Paper [30] proposed a multilevel converter with an adjustable voltage gain, which can decrease the voltage stress and loss of the components. However, the voltage gain is relatively low, and the control and drive circuit is complex. A high step-up DC/DC converter has been proposed [31] in which both voltage and current stresses of components can be adjusted; however, the number of input phase and voltage multiple must satisfy a fixed relationship to realise the equal current of each phase.

This paper presents a novel topology based on scalable voltage multiple cell (SVMC) for high-power applications to solve the problem of high-current stress on components or complex current-balance strategies in the above converters. The property characteristics and some comparisons about LV–MV converters are given in Section 2. Then, a 2.5 MW simulation model and 1.2 kW prototype were constructed for verifying in Sections 3 and 4. The conclusion shows that the proposed converter can reduce the current stress of the components by adjusting the input phase number with the capacity of automatic input-current sharing. Moreover, the voltage stress of the insulated-gate bipolar transistors (IGBTs) and diodes can be effectively reduced by adjusting the number of SVMCs.

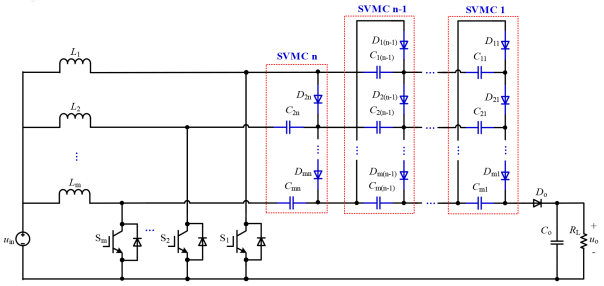


Fig. 2 *Topology of the proposed high step-up SVMC-based DC/DC converter*

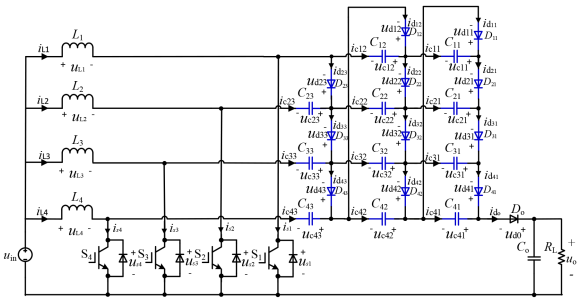


Fig. 3 *Topology of the proposed DC/DC converter with four input phases and three SVMCs*

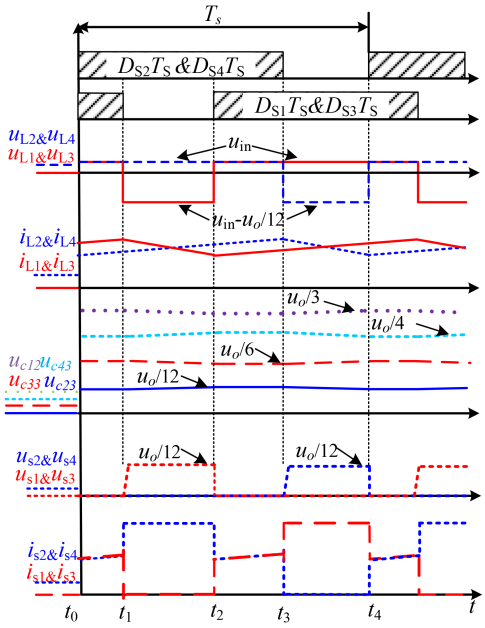


Fig. 4 *Main waveforms in one switching period*

2 Topology and performance analysis

2.1 General topology

The proposed converter topology is composed of one output diode D_o, one output filter capacitor C_o, m inductors, m IGBTs and n SVMCs as shown in Fig. 2. From the beginning of SVMC1 to SVMC $n-1$, the structure of these SVMCs are completely identical, which includes m capacitors and m diodes. SVMC n includes $m-1$ capacitor and $m-1$ diode. The number of input ports of SVMC is defined by input phases. Moreover, the number of SVMCs can be adjusted according to the application demand to the voltage conversion ratio.

2.2 Operation principle

Fig. 3 shows the proposed converter which consists of four input phases and three SVMCs, for example, to analyse its working principle. To simplify the analysis process, all processes of analysis are assumed as follows:

(i) The inductor currents i_{L1}, i_{L2}, i_{L3}, i_{L4} are continuous.
(ii) Ignore the voltage ripple on capacitors.
(iii) All components are ideal and neglect the influence of parasitic parameters.
(iv) The duty cycles of all switches are identical and larger than 0.5, control signals of switches S_1, S_3 and S_2, S_4 are interleaved with 180°.

The converter has three operational stages in one switching period T_s. Main waveforms and equivalent circuits are shown in Figs. 3 and 4 (in Fig. 4, $D=0.7$), where D_{S1}, D_{S2}, D_{S3}, D_{S4} represent the control signals of S_1, S_2, S_3, S_4, respectively:

State 1 [t_0–t_1, t_2–t_3] (Fig. 5a): During this stage, S_1, S_2, S_3, S_4 are working on on state, all diodes are blocked, the inductor currents i_{L1}, i_{L2}, i_{L3}, i_{L4} are rising linearly, all capacitor voltages in SVMC remain constant, output voltage u_o is decreasing. This stage ends when S_1, S_3 are turned off at t_1.

State 2 [t_1–t_2] (Fig. 5b): S_1 and S_3 are turned OFF at t_1. During this stage, S_2, S_4 remains working on on state, diodes D_{21}, D_{22}, D_{23}, D_{41}, D_{42}, D_{43} are turned on, D_o, D_{11}, D_{12}, D_{31}, D_{32}, D_{33} remain working on off state, inductor currents i_{L2} and i_{L4} are rising linearly, i_{L1} and i_{L3} are declining linearly. This stage ends when switches S_1, S_3 are turned on at t_2.

State 3 [t_3–t_4] (Fig. 5c): S_2 and S_4 are turned OFF at t_3. During this stage, S_1, S_3 remain working on on state, diodes D_o, D_{11}, D_{12}, D_{31}, D_{32}, D_{33} are turned on. Diodes D_{21}, D_{22}, D_{23}, D_{41}, D_{42}, D_{43} working on off state, inductor currents i_{L1} and i_{L3} are rising linearly and i_{L2} and i_{L4} are declining linearly. This stage ends when switches S_2, S_4 are switched on at t_4.

Suppose the average current of the inductor L_1–L_4 are set as I_{L1}, I_{L2}, I_{L3} and I_{L4}. Neglecting the ripple of the input current i_{in} and set its average value as I_{in}. By the employing ampere-second balance on capacitors C_{23}, C_{33}, C_{43}, the following equations can be obtained by:

$$\begin{cases} I_{L4}(1-D)T_s = I_{L3}(1-D)T_s \\ I_{L3}(1-D)T_s = I_{L2}(1-D)T_s \\ I_{L2}(1-D)T_s = I_{L1}(1-D)T_s \end{cases} \quad (1)$$

Owing to

$$I_{L1} + I_{L2} + I_{L3} + I_{L4} = I_{in} \tag{2}$$

From (1) and (2), average current stresses of inductors L_1, L_2, L_3 and L_4 can be expressed as

$$I_{L1} = I_{L2} = I_{L3} = I_{L4} = \frac{1}{4} I_{in} \tag{3}$$

On the basis of the capacitor ampere-second balance principle, when the converter works in a steady state, the average current of the capacitors during one switch period is zero, so all diodes in Fig. 3 have the same average current as I_{Dall}

$$I_{Dall} = \frac{1}{12} I_{in}(1 - D) \tag{4}$$

The average current stresses of switches S_1, S_2, S_3 and S_4 are denoted as I_{s1}, I_{s2}, I_{s3} and I_{s4}, respectively, as

$$\begin{cases} I_{s1} = DI_{L1} + (1 - D)I_{L4} - I_{Do} \\ I_{s2} = DI_{L2} + (1 - D)I_{L1} \\ I_{s3} = DI_{L3} + (1 - D)I_{L2} \\ I_{s4} = DI_{L4} + (1 - D)I_{L3} \end{cases} \tag{5}$$

From (4) and (5), the average currents of S_1, S_2, S_3 and S_4 can be expressed as

$$\begin{cases} I_{s1} = \dfrac{2 + D}{12} I_{in} \\ I_{s2} = I_{s3} = I_{s4} = \dfrac{1}{4} I_{in} \end{cases} \tag{6}$$

Similarly, the current stresses of the above components in a general topology which consists of m input phases and n SVMCs can be given by

$$I_{L1} = I_{L2} = \cdots I_{Lm} = \frac{1}{m} I_{in} \tag{7}$$

$$I_{Do} = I_{D11} = \cdots I_{Dmn} = \frac{1}{mn} I_{in}(1 - D) \tag{8}$$

$$\begin{cases} I_{s1} = \dfrac{n - 1 + D}{mn} I_{in} \\ I_{s2} = \cdots I_{sm} = \dfrac{1}{m} I_{in} \end{cases} \tag{9}$$

Obviously, the semiconductor current stress has been greatly reduced by expanding the input phases and SVMCs, while the inductor current in each input phase is equal to achieve automatic input-current sharing.

2.3 Voltage conversion gain

On the basis of the principle of voltage-second balance of inductors L_1–L_4, the following equations can be deduced:

$$L_1 \begin{cases} u_{in}D = (u_{c23} - u_{in})(1 - D) \\ u_{in}D = (u_{c22} - u_{c12} + u_{c23} - u_{in})(1 - D) \\ u_{in}D = (u_{c21} - u_{c11} - u_{c12} + u_{c22} + u_{c23} - u_{in})(1 - D) \end{cases} \tag{10}$$

$$L_2 \begin{cases} u_{in}D = (u_{c33} - u_{c23} - u_{in})(1 - D) \\ u_{in}D = (u_{c32} - u_{c22} - u_{c23} + u_{c33} - u_{in})(1 - D) \\ u_{in}D = (u_{c31} - u_{c21} - u_{c22} - u_{c23} + u_{c32} + u_{c33} \\ \qquad - u_{in})(1 - D) \end{cases} \tag{11}$$

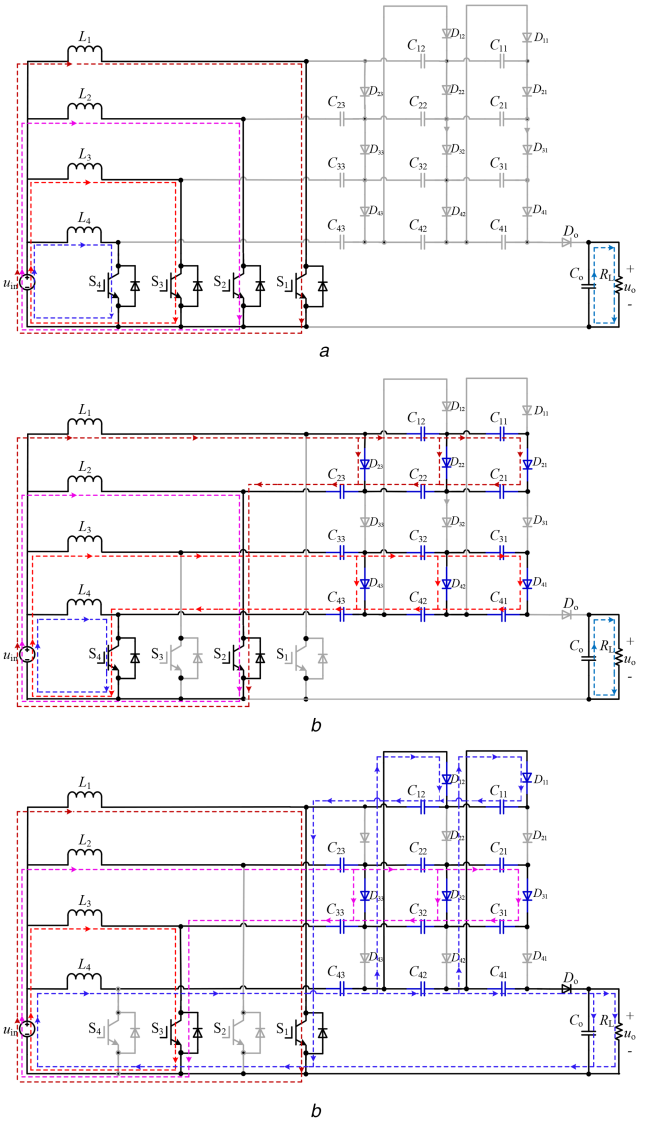


Fig. 5 *Equivalent circuits of each state*
(a) State 1, ***(b)*** State 2, ***(c)*** State 3

$$L_3 \begin{cases} u_{in}D = (u_{c43} - u_{c33} - u_{in})(1 - D) \\ u_{in}D = (u_{c42} - u_{c32} - u_{c33} + u_{c43} - u_{in})(1 - D) \\ u_{in}D = (u_{c41} - u_{c31} - u_{c32} - u_{c33} + u_{c42} + u_{c43} \\ \qquad - u_{in})(1 - D) \end{cases} \tag{12}$$

$$L_4 \begin{cases} u_{in}D = (u_{c12} - u_{c43} - u_{in})(1 - D) \\ u_{in}D = (u_{c11} - u_{c42} - u_{c43} + u_{c12} - u_{in})(1 - D) \\ u_{in}D = (u_{co} - u_{c41} - u_{c42} - u_{c43} - u_{in})(1 - D) \end{cases} \tag{13}$$

From (10) to (13), the following equations are given by:

$$u_{c23} = \frac{u_{in}}{1 - D} \tag{14}$$

$$u_{c33} = 2u_{c23} = \frac{2u_{in}}{1 - D} \tag{15}$$

$$u_{c43} = 3u_{c23} = \frac{3u_{in}}{1 - D} \tag{16}$$

$$u_o = \frac{12u_{in}}{1 - D} \tag{17}$$

The voltages of other capacitors are equal which can be calculated by

Table 1 Performance comparison

Parameters	Proposed one	Paper [11]	Paper [28]	Paper [29]	Paper [30]
voltage conversion gain	$\frac{mn}{1-D}$	$m+n+1$	$2^{n+1}-1$	$\frac{n}{1-D}$	$\frac{1+D}{1-D}$
voltage stress of switches	$\frac{u_{in}}{1-D}$	u_{in}	$2u_{in}$	$\frac{u_{in}}{1-D}$	$\frac{u_{in}}{3(1-D)}$
voltage stress of diodes	$\frac{2u_{in}}{1-D}$	u_{in}	$3u_{in}$	$\frac{u_{in}}{1-D}$	$\frac{u_{in}}{3(1-D)}$
current stress of switches	$\frac{1}{m}I_{in}$	$\frac{6\pi}{m+n+1}I_{in}$	$\frac{4\pi}{2^{n+1}-1}I_{in}$	$\frac{n-1+D}{n}I_{in}$	$\frac{2D}{1+D}I_{in}$
current stress of diodes	$\frac{1-D}{mn}I_{in}$	$\frac{\pi}{m+n+1}I_{in}$	$\frac{2\pi}{2^{n+1}-1}I_{in}$	$\frac{1-D}{n}I_{in}$	$\frac{1-D}{1+D}I_{in}$
automatic input-current sharing	yes	no	yes	no	no

Table 2 Parameters of simulation model

Parameter	Value
input voltage	1 kV
output voltage	40 kV
output power	2.5 MW
switching frequency	5 kHz
IGBT module	5SNE0800E330100
diode module	RM250DG-130 F
inductor	880 μH
third SVMC capacitor C63	338 μF
third SVMC capacitor C53	426 μF
third SVMC capacitor C43	568 μF
third SVMC capacitor C33	852 μF
third SVMC capacitor C23	1704 μF
second SVMC capacitors	188 μF
first SVMC capacitors	94 μF
output filter capacitor	172 μF
duty cycle	0.55%

$$u_{C\,other} = \frac{4u_{in}}{1-D} \tag{18}$$

Therefore, the voltage conversion gain is presented as

$$M = \frac{u_o}{u_{in}} = \frac{12}{1-D} \tag{19}$$

Similarly, the voltage conversion gain and semiconductor components voltage stress of the proposed converter in a general topology which consists of m input phases and n SVMCs can be given by

$$\begin{cases} M = \dfrac{mn}{1-D} \\ u_{S-stress} = \dfrac{u_{in}}{1-D} \\ u_{D-stress} = \dfrac{2u_{in}}{1-D} \quad \left(\text{except:} u_{Do-stress} = \dfrac{u_{in}}{1-D}\right) \end{cases} \tag{20}$$

2.4 Component stress analysis and comparison

The voltage stress on IGBTs and output diode D_o in the proposed converter are equal as shown in (20), and the voltage stresses on other diodes are twice of the output diode D_o. Table 1 shows the comparison of voltage stress, current stress and other performances between the proposed converter and the converter in the papers [11, 28–30], where I_{in} is the input average current and u_{in} is the input voltage. Although the number of input phase in the paper [11] can be controlled, the automatic input-current sharing cannot be achieved between each phase. The converter proposed in paper [28] can both achieve an adjustable input phase and automatic input-current sharing, but the voltage stress of the semiconductor devices cannot be adjusted. The input-port number of the converter proposed in paper [29] is constant. Therefore, many modules are required to work in parallel in high-power applications, which make the system to be more expensive and complex. The voltage conversion gain of the converter in the paper [30] is relatively low than others, which make it difficult to apply in high step-up occasions.

3 Optimisation and simulation

3.1 Optimisation of the proposed converter

The proposed converter has the features of adjustable voltage and current stress on the components and voltage conversion gain according to the number of input phases and SVMCs. It is very important to optimise the circuit topology considering not only efficiency, but also cost. Optimisation results of the proposed converter are given below based on EV-100 wind turbine and the working environment is set as shown in Table 2. All inductor peak-to-peak current ripple is set to be 30% of its DC value, all capacitor peak-to-peak voltage ripple of SVMCs is set to be 1% of its DC value and output voltage peak-to-peak ripple is set to be 0.1% of its DC value. The constraints of the optimal design include: (i) the duty cycle of switches has to be between 0.55 and 0.75. (ii) There are commercially available semiconductor components to satisfy design requirements such as voltage and current stresses.

After considering the above restrictions, the possible options of input phases or SVMCs are shown in Table 3.

The designs of the switches, diodes, inductors and capacitors of each case in Table 3 have been optimised at different switching frequencies, then the efficiency and cost of the converter are analysed and shown in Fig. 6. Fig. 6*a* shows the relationship between the cost, efficiency and switching frequency of the proposed converter for different input phases and SVMCs. To

Table 3 Possible options of input phases or SVMCs

Number of input phases and SVMCs	D	V_S, V	I_S, A	IGBT	Diode	$f_{s\text{-}max}$, kHz
$m = 4$, $n = 4$	0.6	3250	813	5SNE100 0E330300	RM250DG-130F	19.4
$m = 6$, $n = 3$	0.55	2889	542	5SNE 080 0E330100		23.6
$m = 8$, $n = 2$	0.6	3250	407	5SNG 045 0X330300		33.2
$m = 16$, $n = 1$	0.6	3250	203	5SNG 025 0P330305		24.3
$m = 18$, $n = 1$	0.55	2889	181	5SNG 025 0P330305		24.3

Note: V_S and I_S are the voltage and current stresses of switches with a 30% safety margin. The possible maximum switching frequency $f_{s\text{-}max}$ in Table 3 only considers the switching times of IGBTs and the influence of other factors has been ignored.

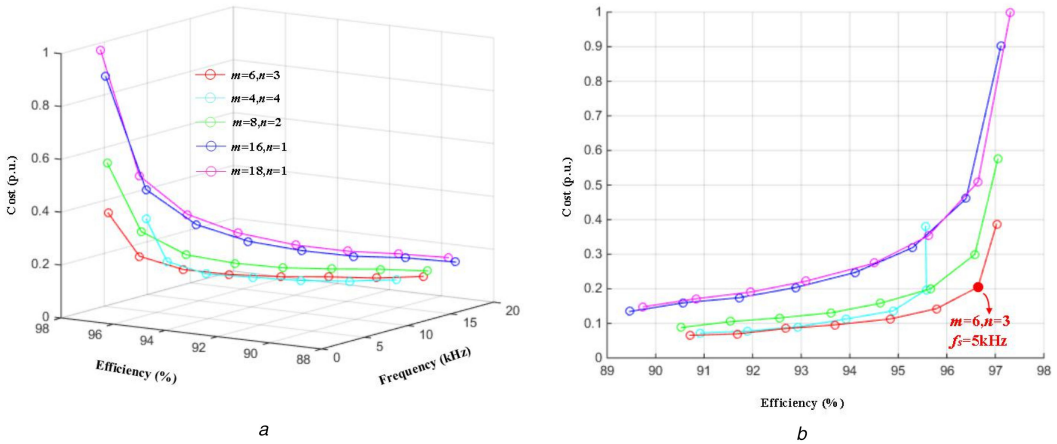


Fig. 6 *Optimisation results*

(a) Three-dimensional graph of cost, efficiency and frequency, ***(b)*** Plane projection graph of cost and efficiency

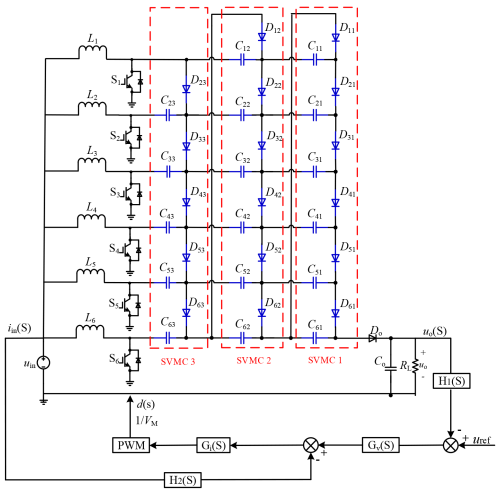


Fig. 7 *Control schematic diagram*

display the results more clearly, Fig. 6*b* is the plane projection graph showing the cost versus efficiency relationship. The optimal selection of the design parameters depends on specific design criteria such as maximum cost, lowest efficiency etc. Here, $m = 6$, $n = 3$ and $f_s = 5$ kHz is selected as the assumed optimised design, after careful consideration on the trade-off between the efficiency and the cost.

A double-loop average current mode-based control strategy has been designed for the proposed converter as shown in Fig. 7. Model and controller design of the proposed converter has been given in the Appendix. Simulation results are shown in Figs. 8 and 9, and Table 2 lists the simulation parameters.

3.2 Simulation results

The gate signals of switches S_1, S_2, S_3, S_4 are denoted as Q_1, Q_2, Q_3 and Q_4 in Fig. 8*a*-1. Fig. 8*a*-2 shows the waveform of the output voltage. Considering the influence of capacitor voltage ripple in each SVMC, the duty cycle of switches S_1, S_2, S_3, S_4 is about 0.551 when the output voltage is 40 kV. Fig. 8*a*-3 shows the voltage waveform across power switches; all switch voltage stresses are near to 2.2 kV. Fig. 8*a*-4 shows the voltage waveform across the diodes D_{24} and D_{34}, which is about 4.4 kV. As can be seen from Fig. 8*a*-5 that the inductor currents are ~417 A and automatic input-current sharing has achieved between each phase. The current waveforms of IGBTs and D_{24} and D_{34} are presented in Figs. 8*a*-6 and *a*-7, respectively.

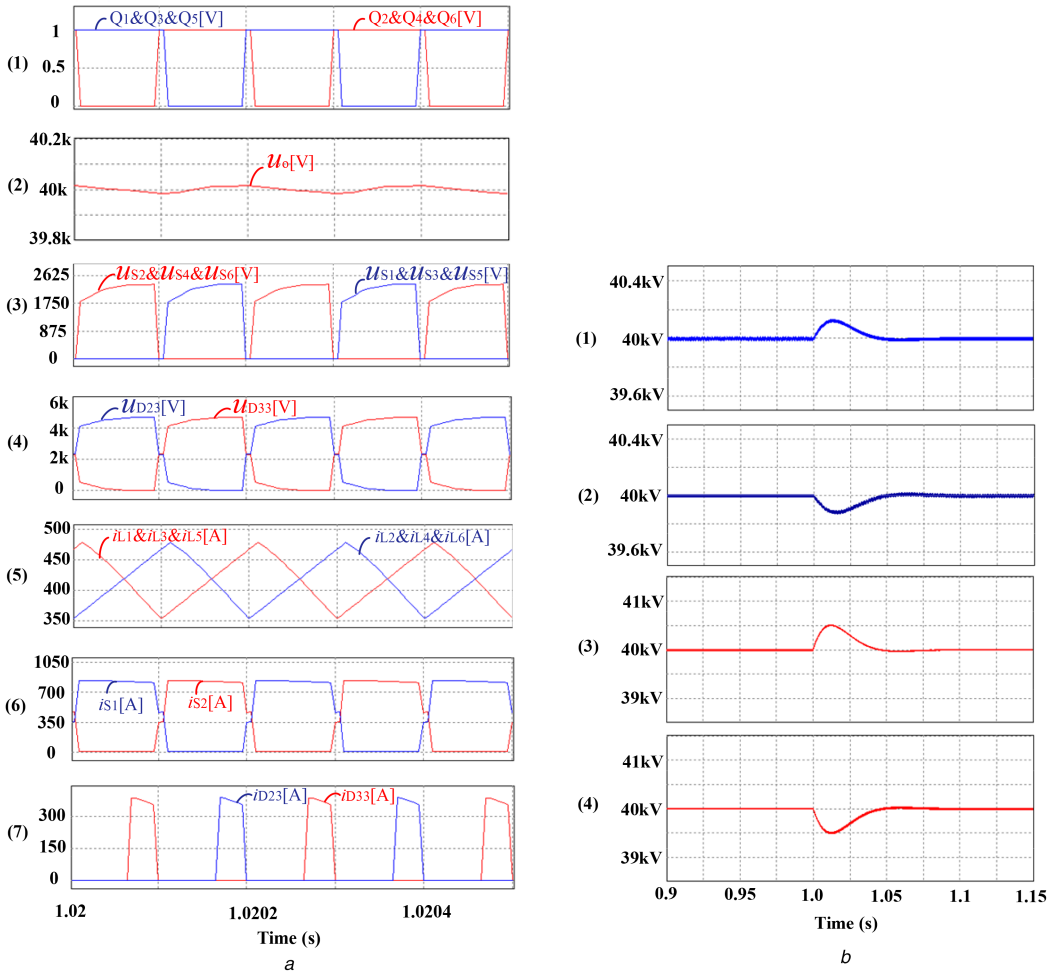


Fig. 8 *Simulation results*
(a) Steady-state simulation waveform, ***(b)*** Dynamic simulation waveform

Figs. 8*b*-1 and *b*-2 show the output voltage response when the input voltage changes from 800 to 1000 V and 1000 to 800 V, respectively. The dynamic response time is about 50 ms when the input voltage is changed at 1 s. The simulation waveforms of the output voltage response are shown in Figs. 8*b*-3 and *b*-4 when the load changes from 2.5 to 1.25 MW and 1.25 to 2.5 MW, dynamic response time is about 100 ms when the output power changes at 1 s.

4 Experimental verification

The proposed converter with four input phases and three SVMCs has been implemented on a 1.2 kW prototype. Table 4 lists the experimental parameters and Fig. 9 shows the experimental results.

The control signals of IGBTs S_1, S_2, S_3, S_4 are denoted as Q_1, Q_2, Q_3 and Q_4 which are shown in Fig. 9*a* and the duty cycle is about 0.7. Fig. 9*b* shows waveforms of input and output voltages. Owing to the error of the sampling circuit, when u_{in} is 30 V, the output voltage u_o is about 1.24 kV, which is slightly higher than the set value of 1.2 kV. The voltage waveforms across switches are shown in Fig. 9*c*, which are close to 100 V. The voltage stresses of third SVMC diodes are about 200 V which is twice of output diode as shown in Fig. 9*d* which is consistent with (20). The voltages waveform of the third SVMC capacitors is shown in Fig. 9*e*, where u_{c23} is ∼100 V, u_{c33} is ∼200 V and u_{c43} is ∼300 V. The current of each input phase is ∼10 A which is shown in Fig. 9*f* and automatic input-current sharing has been achieved between each phase. The currents of the IGBTs and diodes are shown in Figs. 9*g* and *h*. Apparently, all results correspond to the theoretical analysis in Section 2. Dynamic tests of the prototype are shown in Figs. 9*i*–*l*, which shows fast and robust performance for disturbances of load and input voltage.

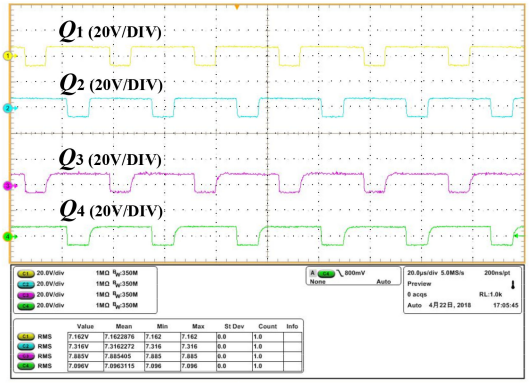
The loss of each part in the prototype can be obtained by calculation according to [32], the loss distribution is shown as Fig. 10*a*. The efficiency curve of the prototype is expressed as Fig. 10*b*. About 93% maximum efficiency of the prototype could be achieved when the output power equals to 1.2 kW.

5 Conclusion

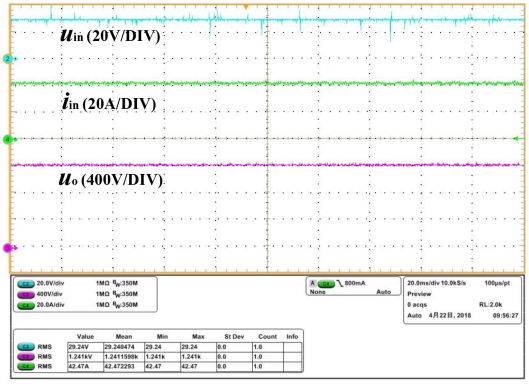
A high step-up SVMCs-based DC/DC converter is proposed in this paper. Theoretical analysis and experimental results show that: (i) both component current and voltage stresses can be adjusted by changing the number of input phase m and SVMC n; (ii) each input phase can automatically achieve current sharing; and (iii) the control and driver circuit is simple. Above characteristics make the proposed converter very suitable for high step-up voltage conversion and high-power applications such as the DC collection grids for offshore wind farms.

6 Acknowledgment

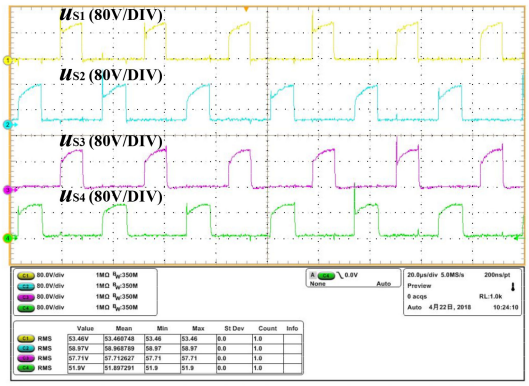
This project was supported by the National Natural Science Foundation of China (51707103).


Q_1 (20V/DIV)
Q_2 (20V/DIV)
Q_3 (20V/DIV)
Q_4 (20V/DIV)

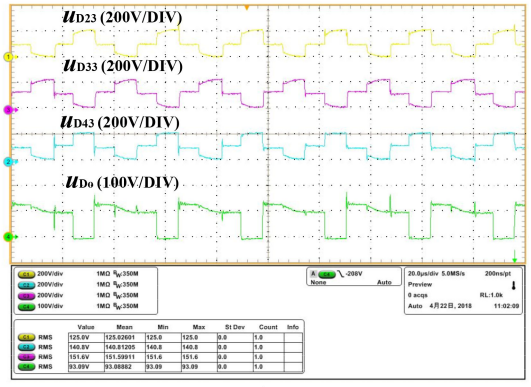
a


u_{in} (20V/DIV)
i_{in} (20A/DIV)
u_o (400V/DIV)

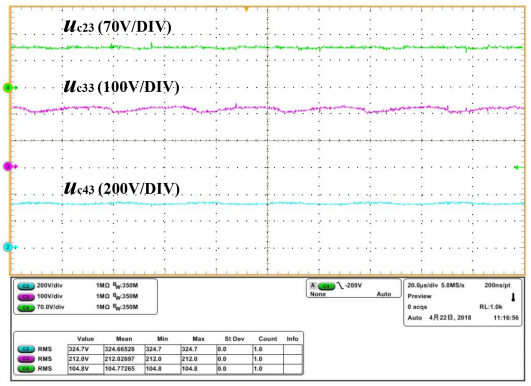
b


u_{S1} (80V/DIV)
u_{S2} (80V/DIV)
u_{S3} (80V/DIV)
u_{S4} (80V/DIV)

c


u_{D23} (200V/DIV)
u_{D33} (200V/DIV)
u_{D43} (200V/DIV)
u_{Do} (100V/DIV)

d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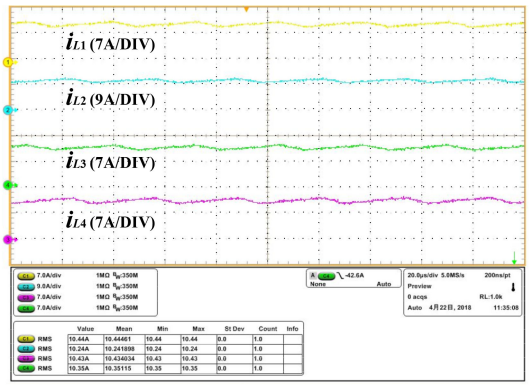
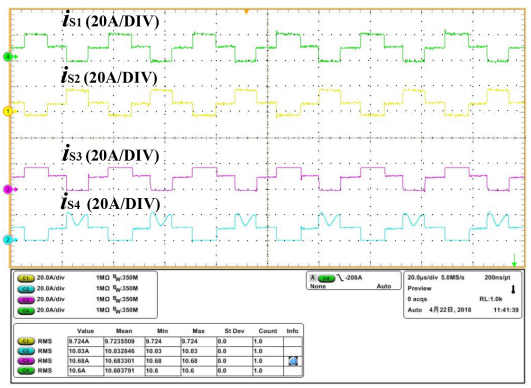
u_{c33} (100V/DIV)
u_{c43} (200V/DIV)

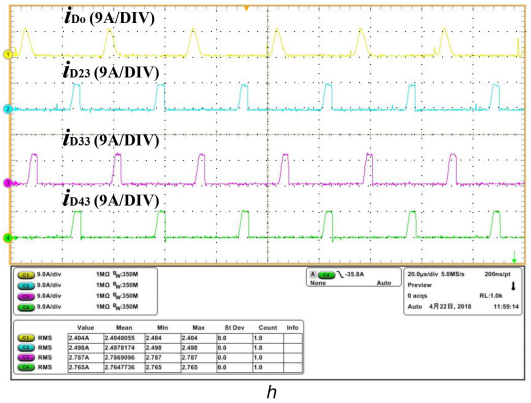
e


i_{L1} (7A/DIV)
i_{L2} (9A/DIV)
i_{L3} (7A/DIV)
i_{L4} (7A/DIV)

f


i_{S1} (20A/DIV)
i_{S2} (20A/DIV)
i_{S3} (20A/DIV)
i_{S4} (20A/DIV)

g


i_{Do} (9A/DIV)
i_{D23} (9A/DIV)
i_{D33} (9A/DIV)
i_{D43} (9A/DIV)

h

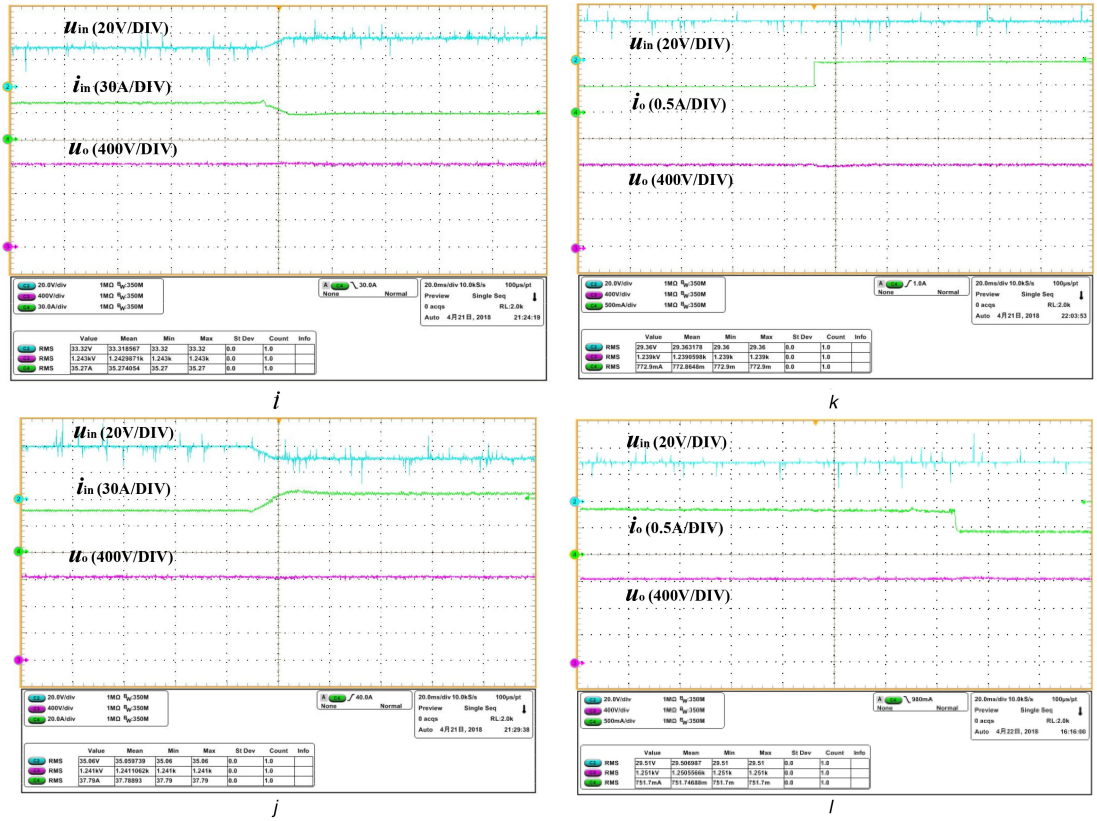


Fig. 9 *Experimental waveforms*

(a) Driver signals of each switch, ***(b)*** Input and output voltages, ***(c)*** Voltage across switches, ***(d)*** Voltage across diode, ***(e)*** Voltage across the third SVMC capacitor, ***(f)*** Current across inductors, ***(g)*** Current across switches, ***(h)*** Current across the third SVMC diode and D_O, ***(i)*** Input voltage change from 30 to 40 V, ***(j)*** Input voltage change from 40 to 30 V, ***(k)*** Output power change from 600 to 1200 W, ***(l)*** Output power change from 1200 to 600 W

Table 4 Parameters of experimental prototype

Parameter	Value/device model
IGBT module	IRGP4055DPbF
diode module	IDT12S60
inductors	800 μH/KS226-125A*2
SVMC capacitor C_{23}	60 μF/STH-250-30*2
SVMC capacitors C_{33}, C_{43}	10 μF/STH-600-10
SVMC capacitors C_{12}, C_{22}, C_{32}, C_{42}, C_{11}, C_{21}, C_{31}, C_{41}	10 μF/KD8102K505*2
output filter capacitor	33 μF/SHP-4000-33
input voltage	30 V
output voltage	1.2 kV
duty cycle	70%
switching frequency	30 kHz
output power	1.2 kW

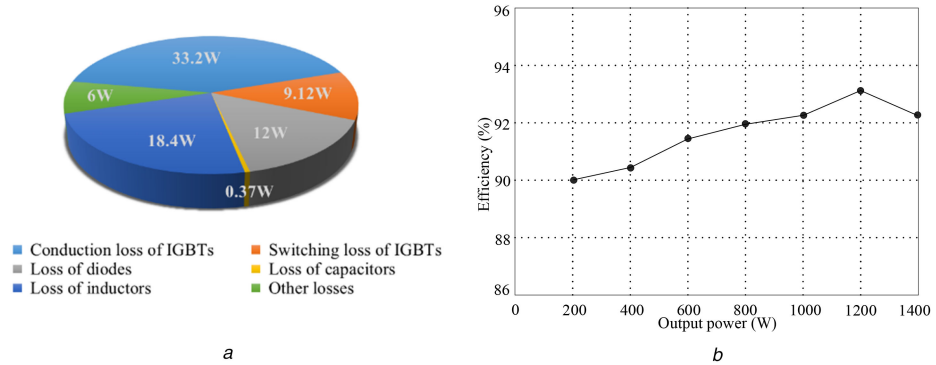


Fig. 10 *Efficiency analysis*

(a) Losses distribution, ***(b)*** Efficiency curve

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8 Appendix

8.1 Model of the proposed converter

On the basis of (14)–(18), the voltage of the capacitors in SVMCs is treated as a voltage-controlled voltage source, which satisfies the equation below:

$$\begin{cases} u_{c23}(t) = \dfrac{1}{18} \cdot u_o(t) \\ u_{c33}(t) = \dfrac{2}{18} \cdot u_o(t) \\ u_{c43}(t) = \dfrac{3}{18} \cdot u_o(t) \\ u_{c53}(t) = \dfrac{4}{18} \cdot u_o(t) \\ u_{c63}(t) = \dfrac{5}{18} \cdot u_o(t) \\ u_{c12}(t) = \cdots u_{c61}(t) = \dfrac{6}{18} \cdot u_o(t) \end{cases} \tag{21}$$

Taking all the inductor current (i_{in}) and output voltage (u_o) as state variables, and using the state-space averaging method for one switching period T_s, the state equation can be given as in the equation below:

$$\begin{cases} L_{eq}\dfrac{d\langle i_{in}(t)\rangle_{Ts}}{dt} = \langle u_{in}(t)\rangle_{Ts} - d'(t)\dfrac{1}{18}\langle u_o(t)\rangle_{Ts} \\ C_o\dfrac{d\langle u_o(t)\rangle_{Ts}}{dt} = d'(t)\dfrac{1}{18}\langle i_{in}(t)\rangle_{Ts} - \dfrac{\langle u_o(t)\rangle_{Ts}}{R} \end{cases} \tag{22}$$

From (22), the average model equivalent circuit of the proposed converter is shown in Fig. 11, where the control variable is $d(t)$, and $d'(t) = 1 - d(t)$, and the state variable to be controlled is the output voltage u_o.

Performing small-signal perturbation at given equilibrium point as shown in Table 2 and ignoring the high-order infinitesimals, averaged small-signal ac model for the proposed converter can be given in the equation below:

$$\begin{cases} L_{eq}\dfrac{d\hat{i}_{in}(t)}{dt} = \hat{u}_{in}(t) + \hat{d}(t)\dfrac{u_o}{18} - \dfrac{D'}{18}\hat{u}_o(t) \\ C_o\dfrac{d\hat{u}_o(t)}{dt} = -\hat{d}(t)\dfrac{I_{in}}{18} + D'\dfrac{\hat{i}_{in}(t)}{18} - \dfrac{\hat{u}_o(t)}{R} \end{cases} \tag{23}$$

The control-to-output voltage and control-to-input-current transfer functions are as follows:

$$G_{ud}(s) = \frac{D'u_oR - 18SLRI_{in}}{216S^2LC_oR + 216SL + D'^2R} \tag{24}$$

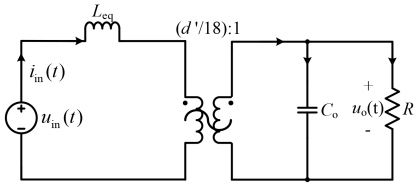

Fig. 11 *Average model equivalent circuit of the proposed converter*

$$G_{id}(s) = \frac{18Su_oC_oR + 18u_o + I_{in}D'R}{216S^2LC_oR + 216SL + D'^2R} \quad (25)$$

8.2 Controller design

The control-to-output transfer function of the proposed converter has a right-half-plane zero which makes it very difficult to achieve good closed-loop performance with single-loop control. Since the crossover frequency of the open-loop system is severely restricted by the right-half-plane zero, a double-loop control scheme has been implemented for switching regulators by sensing the input-current state and using it for feedback together with the output voltage as shown in Fig. 7. For the parameters of $V_M = 1$, $H_1(s) = 10^{-4}$ and $H_2(s) = 10^{-2}$, (26) gives the current loop gain expression before compensation, and its frequency characteristics are shown in Fig. 12*a*. For the current loop compensator of (27), the Bode diagram of the current loop gain after compensation is shown in Fig. 12*b*

$$T_i = G_{id}(s) \cdot \frac{1}{VM} \cdot H_2(s) \quad (26)$$

$$G_i(s) = \frac{s + 2500\pi}{s} 0.04 \quad (27)$$

Equation (28) is the loop gain of voltage loop before compensation; its amplitude frequency and phase frequency characteristics are shown in Fig. 13*a*. For the voltage loop compensator given in (29), the Bode diagram of the voltage loop gain after compensation is shown in Fig. 13*b*

$$T_v = \frac{G_i(s)\,(1/VM)\,G_{ud}(s)\,H_1(s)}{1 + G_{id}(s)\,(1/VM)\,H_2(s)\,G_i(s)} \quad (28)$$

$$G_v(s) = \frac{s + 2500\pi}{s} \frac{5.9 \times 10^{-3}s + 1}{4.26 \times 10^{-4}s + 1} 10 \quad (29)$$

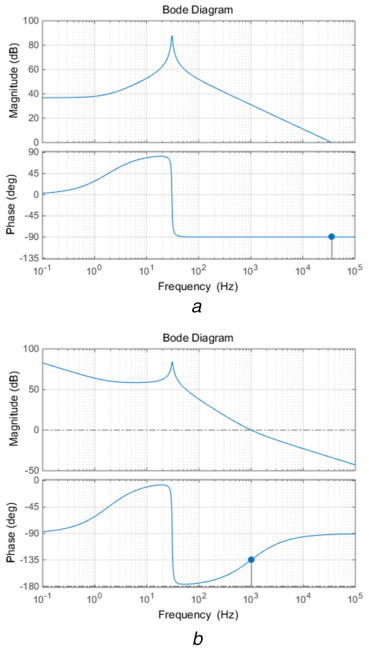

Fig. 12 *Frequency characteristic of the current loop gain* ***(a)*** Before compensation, ***(b)*** After compensation

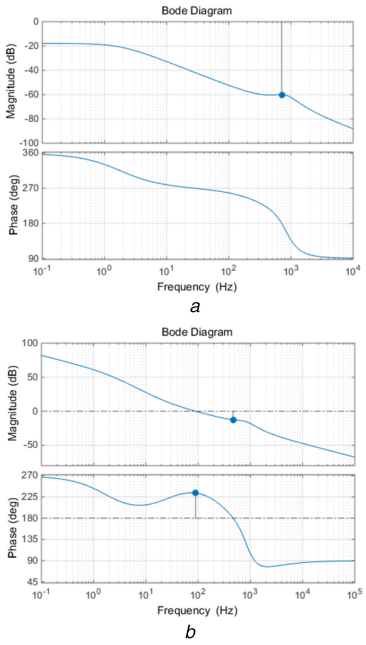

Fig. 13 *Frequency characteristic of the current loop gain* ***(a)*** Before compensation, ***(b)*** After compensation