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A Generic Control-Oriented Model Order Reduction Approach for High Step-Up DC/DC Converters Based on Voltage Multiplier

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Abstract: The modeling and control system design of high step-up DC/DC converters based on voltage multipliers (VMs) are difficult, due to the various circuit topologies and the presence of large number of capacitors in VMs. This paper proposes a generic approach to reduce the model order of such converters by replacing the VM capacitors with voltage sources controlled by the output voltage of the converter. Theoretical analysis and simulation results show that the derived models can accurately represent the low frequency response of the converter which is valuable for obtaining a small-signal AC model for control system design. The detailed modeling and controller design process are demonstrated for the converter, and the obtained simulation results are verified experimentally on a 400 W prototype.

Keywords: DC/DC converter; reduced order model; high step-up converter; voltage multiplier (VM); control system design

1. Introduction

The desire for clean environment, low carbon emission and the fact that fossil fuel reserves are depleting have led to the rapid development of renewable energy generation systems. Renewable energy generating units, such as photovoltaic arrays and wind turbine generators, present lower output voltage compared to the interconnected grid systems, and thus high voltage step-up methods are required for grid integration. It is also important to provide active control to these energy conversion devices in order to maximize the energy harvested, which calls for high-efficiency power electronic converters. High step-up voltage conversion technology based on voltage multiplier (VM) is one of the solutions [1] and has recently become increasingly popular in renewable applications such as solar photovoltaic [2,3], wind power generation [4], and fuel cell power generation [5,6].

In recent years, various VM circuits have been proposed to achieve a family of high step-up non-isolated DC/DC converter topologies for the applications in renewables [7–22]. A generalized circuit structure of a family of non-isolated converters with VM is shown in Figure 1, where the switch/inductor circuit is connected to the diode-capacitor VM to supply the load R_L . The output voltage u_o of the converter can be stepped up to much higher level compared to the input voltage u_{in} . For the diode-capacitor VM circuit, voltage doubler circuit [7], voltage quadrupler circuit [8], Dickson charge pump [9], Cockcroft–Walton VM [10], and amongst others [17] have been used, and based on which various other different VM circuits have been proposed for two-input-phase interleaved booster

converter [5,11–13] and multiple-input-phase booster converter [4,14–16,19]. Coupled-inductor has been used to replace the inductors to provide further performance improvement [6,23,24].

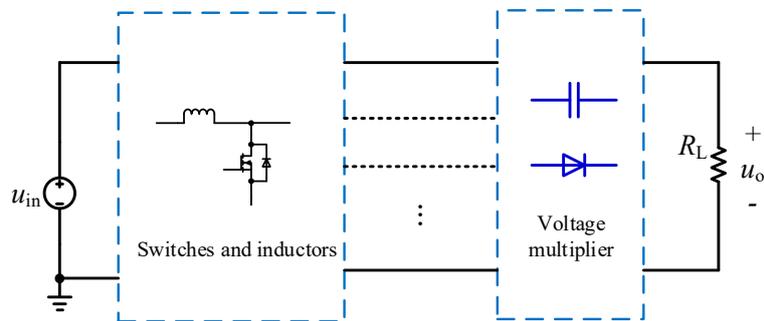


Figure 1. A general circuit for a family of non-isolated high step-up DC/DC converter with capacitor-diode VM.

However, most of the existing literature on this type of converter focus on derivation of the circuit topology and/or design optimization, while the determination of the control structure and the tuning of the control parameters are simply based on empirical methods, or even not discussed. The lack of systematic approach to modeling and control system design will lead to cumbersome parameter tuning process and/or poor performance of the converter, especially under highly-varying conditions of the renewable generations, which can offset the benefits of this type of promising converter. A large number of capacitors are used in VM circuits, which can effectively increase the voltage conversion gain and reduce the voltage stress of the switching devices, but this also leads to a high-order system and makes the classical model-based design of high-performance control system difficult, unless a suitable control-oriented model order reduction approach is developed for practical applications.

Indeed, modeling and model order reduction approaches have been developed for many VM-based converters, such as those with three-state switching cell [25], switch capacitor [26], coupled-inductor [27]. However, the existing approaches are specifically designed for relatively low-order system and they cannot be readily applied to other topologies, especially when the number of VM cells increases. To reduce the effort of control system design for a family of high step-up DC/DC converters based on diode-capacitor VM, for the first time, this paper proposes a novel general method to acquire their averaged-value reduced-order models. The approach uses the concept to replace all the capacitors in the VM with voltage sources controlled by the output voltage of the converter, and the system order is greatly reduced without sacrificing much model accuracy.

The rest of the paper is organized as follows: Detailed procedure of the proposed model-order reduction method is presented in Section 2. Using this proposed method, general small-signal AC models and relevant transfer functions for the converters based on VM are derived in Section 3. Controller design is included in Section 4, where the low frequency response of the proposed reduced-order small signal AC model is found to be in agreement with the simulation results from the circuit model with detailed switching dynamics. The proposed control design method based on the reduced-order model is verified through simulation and experiment in Section 5. The main findings of the work are concluded in Section 6.

2. Proposed Modeling Method and Reduced-Order Models

2.1. Proposed Model Order Reduction Method

For the type of converters as shown in Figure 1, it has been commonly found that by neglecting the effects of ripples, the voltage across each VM capacitor is in linear relationship to the output voltage u_o of the converter [7–22]. Hence, each VM capacitor can be replaced by a controlled voltage source associated with u_o . As the system order is determined by the number of the energy storage

components in the circuit, the corresponding model order can be greatly reduced. Detailed procedure for the proposed model order reduction approach is described as follows:

Step 1: Obtain the steady-state relationship between all VM capacitor voltages and the output voltage $u_o(t)$ according to the results from circuit analysis. The general relationship can be expressed as

$$u_{cn}(t) = k_n \cdot u_o(t) \quad (1)$$

where $u_{cn}(t)$ is the voltage of n -th VM capacitor and k_n is corresponding proportional gain.

Step 2: Replace all VM capacitors, except the ones at the output, with controlled voltage sources according to (1). This step is shown graphically in Figure 2.

Step 3: Reformulate and simplify the resulting model to construct an equivalent reduced-order circuit based on the state-space averaging method [28].

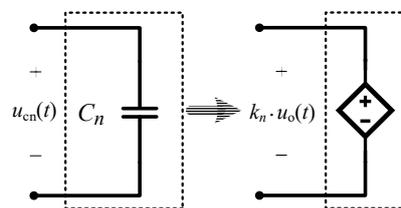


Figure 2. Equivalent circuit of a capacitor where a controlled voltage source is used to replace the VM capacitor.

In this connection, the converter proposed in [12] will be used as an example to demonstrate the proposed approach. Figure 3a shows the topology of this converter with n number of basic VM cells. It consists of two switches S_1 and S_2 , two inductors L_1 and L_2 , and the VM circuits with n VMs. Each VM consists of two diodes and two capacitors with the equal capacitance $C_{ia} = C_{ib} = C_{ik}$ ($i = 1, 2, \dots, n$). The voltage conversion gain is $2n$ times of the traditional boost converter. The driving signals of switches S_1 and S_2 are interleaved and both duty cycles d shall be larger than 0.5. The conversion gain of this converter can be easily adjusted by changing the number of VMs at the design stage. Voltage stress of all semiconductor devices are reduced significantly compared with conventional boost converter, and the two inductor currents can be automatically self-balancing. All capacitors have the same current stress, except the two which are connected with the load, that is, conducive to the thermal design. We denote this converter as the VM converter hereafter in this paper.

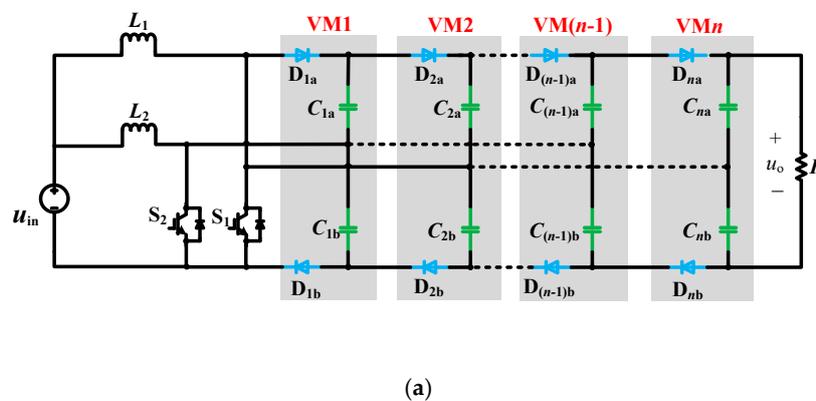


Figure 3. Cont.

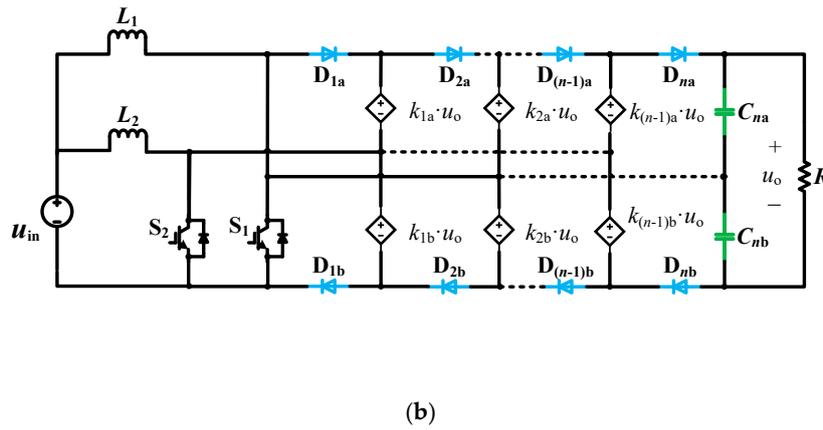


Figure 3. The topology of the VM converter: (a) the original circuit; (b) the modified circuit by replacing capacitors with controlled voltage sources.

The steady-state relationships between the capacitor voltage in VMs and the output voltage are given in (2) based on the analytical results provided in Reference [12]. According to Step 2 of the proposed model order reduction method, the equivalent circuit of this converter by replacing all capacitors in VMs with corresponding controlled voltage sources is shown in Figure 3b.

$$\begin{cases} u_{c1a}(t) = u_{c1b}(t) = \frac{1}{2n} \cdot u_o(t) \\ u_{c2a}(t) = u_{c2b}(t) = \frac{2}{2n} \cdot u_o(t) \\ \dots\dots \\ u_{c(n-1)a}(t) = u_{c(n-1)b}(t) = \frac{n-1}{2n} \cdot u_o(t) \\ u_{cna}(t) = u_{cnb}(t) = \frac{n}{2n} \cdot u_o(t) \end{cases} \quad (2)$$

According to the working state of the switches, the operation mode of this converter can be separated into three regions during one switching period T_S and the equivalent circuits for each region are shown in Figure 4.

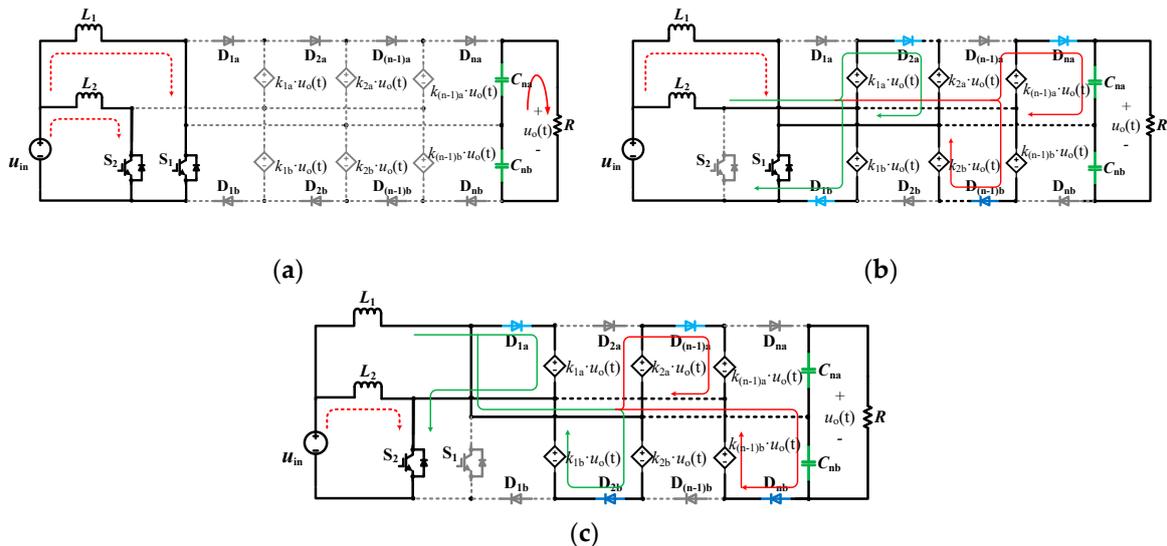


Figure 4. Three working state equivalent circuits of the VM converter: (a) S_1, S_2 are both on; (b) S_1 is on and S_2 is off; (c) S_2 is on and S_1 is off.

Equation (3) can be obtained while S_1 and S_2 are both in on-state. Similarly, (4) is obtained when S_1 is in on-state and S_2 is in off-state. When S_2 is turned-on and S_1 is turned-off, (5) can be obtained.

$$\begin{cases} u_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = u_{in}(t) \\ u_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = u_{in}(t) \\ i_{Cna}(t) = C_{na} \frac{du_{Cna}(t)}{dt} = -\frac{u_o(t)}{R} \\ i_{Cnb}(t) = C_{nb} \frac{du_{Cnb}(t)}{dt} = -\frac{u_o(t)}{R} \\ i_{in}(t) = i_{L1}(t) + i_{L2}(t) \end{cases} \quad (3)$$

$$\begin{cases} u_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = u_{in}(t) \\ u_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = u_{in}(t) - \frac{1}{2n} u_o(t) \\ i_{Cna}(t) = C_{na} \frac{du_{Cna}(t)}{dt} = \frac{1}{n} i_{L2}(t) - \frac{u_o(t)}{R} \\ i_{Cnb}(t) = C_{nb} \frac{du_{Cnb}(t)}{dt} = -\frac{u_o(t)}{R} \\ i_{in}(t) = i_{L1}(t) + i_{L2}(t) \end{cases} \quad (4)$$

$$\begin{cases} u_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = u_{in}(t) - \frac{1}{2n} u_o(t) \\ u_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = u_{in}(t) \\ i_{Cna}(t) = C_{na} \frac{du_{Cna}(t)}{dt} = -\frac{u_o(t)}{R} \\ i_{Cnb}(t) = C_{nb} \frac{du_{Cnb}(t)}{dt} = \frac{1}{n} i_{L1}(t) - \frac{u_o(t)}{R} \\ i_{in}(t) = i_{L1}(t) + i_{L2}(t) \end{cases} \quad (5)$$

Furthermore, according to Reference [12], when the duty cycles of S_1 and S_2 are identical, the average inductor currents of L_1 and L_2 over one switch period T_s shall be equal, i.e.,

$$\langle i_{L1}(t) \rangle_{T_s} = \langle i_{L2}(t) \rangle_{T_s} \quad (6)$$

Next, by replacing the state variables with their low-frequency averaged values over one switch period T_s , (3)–(6) can be simplified to

$$\begin{cases} L_1 \frac{d\langle i_{L1}(t) \rangle_{T_s}}{dt} = \langle u_{in}(t) \rangle_{T_s} - \frac{1}{2n} \langle u_o(t) \rangle_{T_s} \times d'(t) \\ L_2 \frac{d\langle i_{L2}(t) \rangle_{T_s}}{dt} = \langle u_{in}(t) \rangle_{T_s} - \frac{1}{2n} \langle u_o(t) \rangle_{T_s} \times d'(t) \\ C_{na} \frac{d\langle u_{Cna}(t) \rangle_{T_s}}{d(t)} = \frac{1}{n} \langle i_{L2}(t) \rangle_{T_s} \times d'(t) - \frac{\langle u_o(t) \rangle_{T_s}}{R} \\ C_{nb} \frac{d\langle u_{Cnb}(t) \rangle_{T_s}}{d(t)} = \frac{1}{n} \langle i_{L1}(t) \rangle_{T_s} \times d'(t) - \frac{\langle u_o(t) \rangle_{T_s}}{R} \\ \langle i_{in}(t) \rangle_{T_s} = \langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s} \\ \langle i_{L1}(t) \rangle_{T_s} = \langle i_{L2}(t) \rangle_{T_s} \end{cases} \quad (7)$$

where $d' = 1 - d$. Combining (2) and (7) yields the new governing equation of state of the capacitors, i.e.,

$$C_{ia} \frac{d\langle u_{Cia}(t) \rangle_{T_s}}{d(t)} = C_{ib} \frac{d\langle u_{Cib}(t) \rangle_{T_s}}{d(t)} = \frac{i}{n} \cdot \left[\frac{1}{2n} \langle i_{in}(t) \rangle_{T_s} \times d'(t) - \frac{\langle u_o(t) \rangle_{T_s}}{R} \right] \quad (8)$$

where $1 \leq i \leq n - 1$.

Hence, the reduced-order model for the VM converter is obtained as (7) and (8). Based on (7) and (8), its equivalent circuit can be obtained as shown in Figure 5a. It can be clearly seen that the voltage is stepped up through n stages by using n ideal transformers. In the first stage the voltage increases by a factor of $2/d'(t)$, and later the voltage increases linearly. Indeed, by combining the

inductors, the capacitors and the ideal transformers respectively, Figure 5a can be readily simplified to Figure 5b, where the equivalent parameters A and L_{eq} can be readily obtained as

$$A = 2n \tag{9}$$

$$L_{eq} = \frac{L_1 \cdot L_2}{L_1 + L_2} \tag{10}$$

Considering that $C_{ia} = C_{ib} = C_{ik}$, the equivalent capacitance $C_{eq,i}$ of the i -th stage in Figure 5a referring to the final (n -th) stage is

$$C_{eq,i} = \left(\frac{i}{i+1} \cdot \frac{i+1}{i+2} \cdots \frac{n-1}{n} \right)^2 \cdot \frac{C_{ia} \cdot C_{ib}}{C_{ia} + C_{ib}} = \left(\frac{i}{n} \right)^2 \cdot \frac{C_{ik}}{2}$$

Hence, the equivalent C_{eqo} in Figure 5b can be calculated by

$$C_{eqo} = \sum_{i=1}^n C_{eq,i} = \sum_{i=1}^n \left[\left(\frac{i}{n} \right)^2 \cdot \frac{C_{ik}}{2} \right] \tag{11}$$

If $C_{1k} = C_{2k} = \dots C_{nk} = C_k$, and considering, Equation (11) can be further reduced to

$$C_{eqo} = \frac{1}{n^2} \cdot \frac{(n+1)(2n+1)}{6} \cdot \frac{C_k}{2} = \frac{(n+1)(2n+1)}{12n} C_k$$

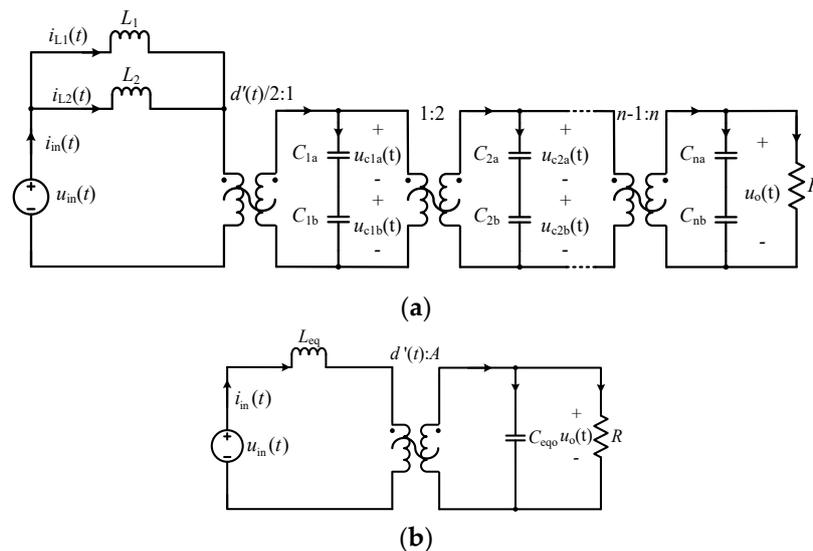


Figure 5. (a) The reduced-order averaged model of the VM converter; (b) The general reduced-order averaged model of the converters based on VM.

2.2. A General Reduced-Order Model of the Converters Based on VM

Using the similar method presented in Section 2.1, the reduced-order averaged models of the existing VM-based converters proposed in References, [9–11,14,16], are investigated and derived. It was found that all the reduced-order models share an identical equivalent circuit structure, as shown in Figure 5b, while the corresponding expressions for parameters L_{eq} , C_{eqo} and A are different; they are summarized in Table 1.

Table 1. Parameters of the reduced-order average model for different converter circuits based on VM.

Ref.	Topology	Expressions of Equivalent Parameters
[9]		$\begin{cases} A = n + 1 \\ L_{eq} = \frac{L_1 \cdot L_2}{L_1 + L_2} \\ C_{eqo} = \sum_{i=1}^n \left(\frac{i}{n+1}\right)^2 \cdot C_i + C_{out} \end{cases}$
[10]		$\begin{cases} A = 2n + 1 \\ L_{eq} = \frac{L_1 \cdot L_2}{L_1 + L_2} \\ C_{eqo} = \sum_{i=1, i \neq 2}^{2n} \left(\frac{2}{2n+1}\right)^2 \cdot C_i \\ + \left(\frac{1}{2n+1}\right)^2 \cdot C_2 + C_{out} \end{cases}$
[11]		$\begin{cases} A = n + 1 \\ L_{eq} = \frac{L_1 \cdot L_2}{L_1 + L_2} \\ C_{eqo} = \sum_{i=1}^{n-1} \left(\frac{2}{n+1}\right)^2 \cdot C_i + \left(\frac{1}{n+1}\right)^2 \cdot C_n + C_o \end{cases}$
[14]		$\begin{cases} A = n + 1 \\ L_{eq} = \frac{1}{\sum_{k=1}^m \left(\frac{1}{L_k}\right)} \\ C_{eqo} = \sum_{j=1}^m \left[\sum_{i=1}^n \left(\frac{1}{n+1}\right)^2 \cdot C_{i,j} \right] + C_o \end{cases}$
[16]		$\begin{cases} A = n \cdot (m - 1) + 1 \\ L_{eq} = \frac{1}{\sum_{k=1}^m \left(\frac{1}{L_k}\right)} \\ C_{eqo} = \sum_{j=1}^{m-1} \left(\frac{j}{n(m-1)+1}\right)^2 \cdot C_{n,j} + \\ \sum_{j=1}^{m-1} \left[\sum_{i=1}^{n-1} \left(\frac{m}{n(m-1)+1}\right)^2 \cdot C_{i,j} \right] + C_o \end{cases}$

3. Small Signal AC Models and Transfer Functions

3.1. Small-Signal AC Models

Based on the state-space averaging method and the proposed reduced-order averaged model as shown in Figure 5, the small-signal AC model of the VM converter can be obtained as

$$\begin{cases} L_{eq} \frac{d\hat{i}_{in}(t)}{dt} = \hat{u}_{in}(t) + \frac{1}{2n} U_o \cdot \hat{d}(t) - \frac{1}{2n} D' \cdot \hat{u}_o(t) \\ C_{eqo} \frac{d\hat{u}_o(t)}{dt} = \frac{1}{2n} D' \cdot \hat{i}_{in}(t) - \frac{1}{2n} I_{in} \cdot \hat{d}(t) - \frac{\hat{u}_o(t)}{R} \end{cases} \quad (12)$$

where I_{in} , U_o and D' are the quiescent values of the input current $i_{in}(t)$, output voltage $u_o(t)$, and $d'(t)$, respectively. $\hat{i}_{in}(t)$, $\hat{u}_o(t)$, $\hat{u}_{in}(t)$ and $\hat{d}(t)$ are the small AC values of the input current $i_{in}(t)$, output voltage $u_o(t)$, input voltage $u_{in}(t)$, and $d'(t)$, respectively.

Using the same method, a general AC small-signal model of the converters based on VM can be obtained, as shown in Figure 6. The expressions of the model parameters including A , B and C , for different topologies, are given in Table 2.

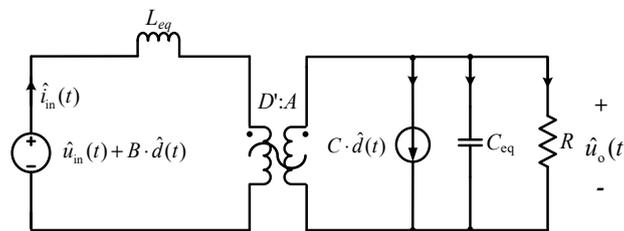


Figure 6. General small-signal AC model of the converters based on VM.

Table 2. Key Parameters of the small-signal AC models for different converter circuits based on VM.

Reference	A	B	C
[12]	$2n$	$\frac{U_o}{2n}$	$\frac{I_{in}}{2n}$
[9,11,14]	$n + 1$	$\frac{U_o}{n+1}$	$\frac{I_{in}}{n+1}$
[10]	$2n + 1$	$\frac{U_o}{2n+1}$	$\frac{I_{in}}{2n+1}$
[16]	$n \cdot (m - 1) + 1$	$\frac{U_o}{n \cdot (m-1) + 1}$	$\frac{I_{in}}{n \cdot (m-1) + 1}$

3.2. Transfer Functions

Based on Figure 6, the general transfer functions related to the controller or filter design of the converters based on VM are derived and given in (13)–(17), where A , B and C for different converter circuits are listed in Table 2.

(1) Control-output voltage transfer function

$$G_{ud}(s) = \frac{\hat{u}_o(s)}{\hat{d}(s)} = \frac{A \cdot B \cdot D' \cdot R - s \cdot A^2 \cdot C \cdot L_{eq} \cdot R}{s^2 \cdot A^2 \cdot L_{eq} \cdot C_{eq} \cdot R + s \cdot A^2 \cdot L_{eq} + D'^2 \cdot R} \quad (13)$$

(2) Line-to-output voltage transfer function

$$G_{ug}(s) = \frac{\hat{u}_o(s)}{\hat{u}_{in}(s)} = \frac{A \cdot D' \cdot R}{s^2 \cdot A^2 \cdot L_{eq} \cdot C_{eq} \cdot R + s \cdot A^2 \cdot L_{eq} + D'^2 \cdot R} \quad (14)$$

(3) Control-input current transfer function

$$G_{id}(s) = \frac{\hat{i}_{in}(s)}{\hat{d}(s)} = \frac{s \cdot A^2 \cdot B \cdot C_{eq} \cdot R + A \cdot C \cdot D' \cdot R + A^2 \cdot B}{s^2 \cdot A^2 \cdot L_{eq} \cdot C_{eq} \cdot R + s \cdot A^2 \cdot L_{eq} + D'^2 \cdot R} \quad (15)$$

(4) Output impedance

$$Z_{out}(s) = \frac{s \cdot L_{eq} \cdot A^2 \cdot R}{s^2 \cdot A^2 \cdot L_{eq} \cdot C_{eq} \cdot R + s \cdot A^2 \cdot L_{eq} + D'^2 \cdot R} \quad (16)$$

(5) Input impedance

$$Z_{in}(s) = \frac{s^2 \cdot A^2 \cdot L_{eq} \cdot C_{eq} \cdot R + s \cdot A^2 \cdot L_{eq} + D'^2 \cdot R}{s \cdot A^2 \cdot C_{eq} \cdot R + A^2} \quad (17)$$

3.3. Accuracy of the Small Signal AC Model

To verify the accuracy and examine the performance of the proposed general small signal AC models and relevant transfer functions of the converters based on VM, a comparison between the proposed models and practical circuits, and controller design of the VM converter, will be presented in this section. The specifications for the simulation are listed in Tables 3 and 4.

The simulation results are shown in Figures 7–9, where the VM numbers are 2, 3, and 5, respectively. The blue line is the actual circuit simulation result using PSIM software, and the red line is the proposed model simulation result obtained from MATLAB R2016a/Simulink 8.7 (The MathWorks, Inc., Natick, MA, USA). When the VM number is 2, Figure 7a,c,e show the output voltage waveforms when the duty cycle changes around 0.6 with different voltage ripple on capacitors in VM due to different C_{na} and C_{nb} . Figure 7b,d,f show the output voltage waveforms when the input voltage changes around 40 V with different voltage ripple on capacitors in VM due to different C_{na} and C_{nb} . It can be seen from Figure 7 that the increase of voltage ripple on capacitor in VM will make the steady-state accuracy of the proposed model worse, but the dynamic response of the proposed model is not affected significantly. When the voltage ripple on capacitors in VM is 10%, Figures 7c, 8a and 9a show the output voltage waveforms when the duty cycle changes around 0.6 with different VM number at $C_{na} = C_{nb} = 2 \mu\text{F}$, while Figures 7d, 8b and 9b show the output voltage waveforms when the input voltage changes around 40 V with different VM number at the same capacitance. Clearly, as the VM number increases, the steady-state error between the proposed model and the actual circuit increases too. This steady-state error is caused by the ripple in the capacitor voltage which affects the converter voltage gain [12].

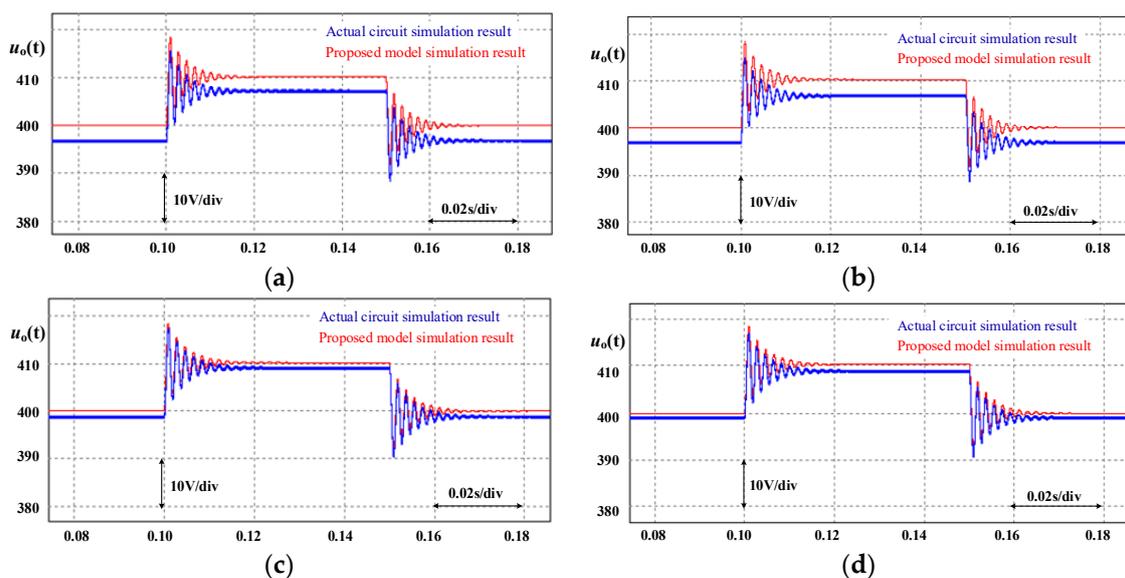


Figure 7. Cont.

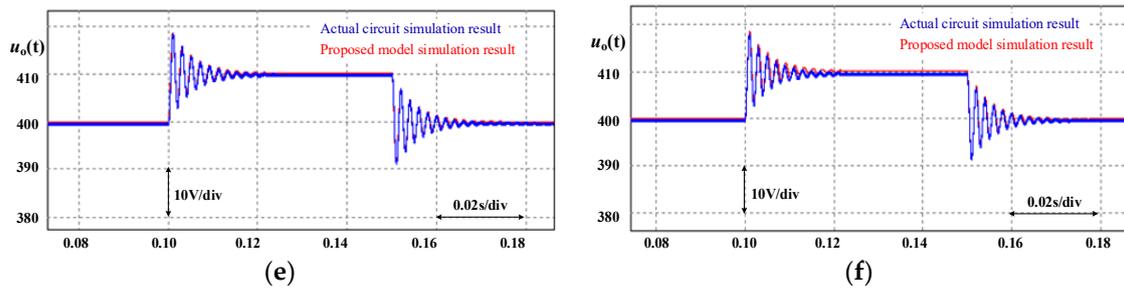


Figure 7. VM number is 2 and (a) $C_{na} = C_{nb} = 0.67 \mu\text{F}$, duty cycle changes; (b) $C_{na} = C_{nb} = 0.67 \mu\text{F}$, input voltage changes; (c) $C_{na} = C_{nb} = 2 \mu\text{F}$, duty cycle changes; (d) $C_{na} = C_{nb} = 2 \mu\text{F}$, input voltage changes; (e) $C_{na} = C_{nb} = 10 \mu\text{F}$, duty cycle changes; (f) $C_{na} = C_{nb} = 10 \mu\text{F}$, input voltage changes.

Table 3. Parameters of Simulation and Experimental Prototype.

Component	Rated Parameters	Extended Parameters
Switches	GP4055	GP4055
Diodes	STTH15L06D	STTH15L06D
VM number	2	3/5
Capacitors in VM (μF)	10	10
Output filter capacitor (μF)	10	10
L_1, L_2 (μH)	320	320
Load resistance (Ω)	400	400
Switch frequency (kHz)	50	50
Duty cycle	0.6	0.6
Input voltage (V)	40	40
Output voltage (kV)	0.4	0.6/1
Output power (kW)	0.4	0.9/2.5

Table 4. Parameters of Capacitor Values with Different VM Numbers.

VM Numbers	Capacitor Values (μF)	Voltage Ripple
2	C_{1a}, C_{1b} : 10	2%
	C_{1a}, C_{1b} : 2	10%
	C_{1a}, C_{1b} : 0.67	30%
3	C_{1a}, C_{1b} : 3	10%
	C_{2a}, C_{2b} : 1.5	
5	C_{1a}, C_{1b} : 5	10%
	C_{2a}, C_{2b} : 2.5	
	C_{3a}, C_{3b} : 1.7	
	C_{4a}, C_{4b} : 1.25	

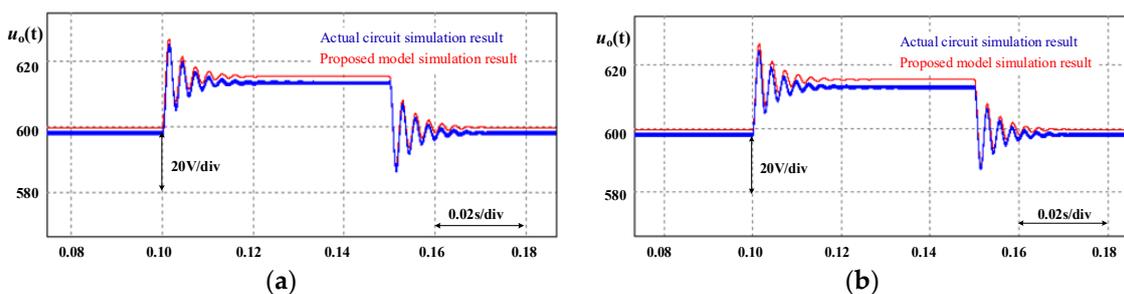


Figure 8. VM number is 3, $C_{na} = C_{nb} = 2 \mu\text{F}$, and (a) duty cycle changes; (b) input voltage changes.

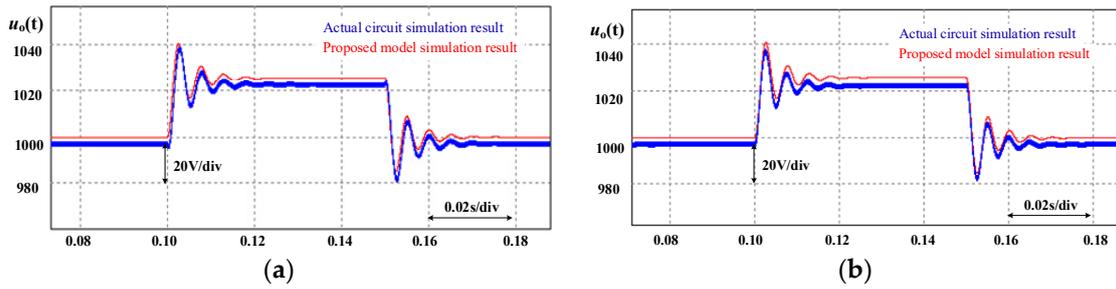


Figure 9. VM number is 5, $C_{na} = C_{nb} = 2 \mu\text{F}$, and (a) duty cycle changes; (b) input voltage changes.

From the above observation, it can be seen that the proposed model will become less accurate in steady-state as the capacitor voltage ripple in VM or the number of VM cells increases. Nevertheless, these negative effects are very limited and negligible for control system design, which can be observed from Figures 7–9. On the other hand, the proposed reduced-order model is capable of capturing the major dynamic characteristics of the detailed circuit model. This can be seen from Figures 7–9, as the dynamic responses are very close. Above characteristics of the proposed reduced order model make it valuable in the controller design of the converter.

4. Controller Design

A voltage and current double-loop control scheme is designed and shown in Figure 10, where $G_v(s)$ and $G_i(s)$ are the transfer functions of the voltage and current regulators respectively. $1/V_M$ is the equivalent gain of the PWM modulator and it is equal to 1.33 V based on the control chip (ISL6558) specifications. Furthermore, $H_1(s)$ and $H_2(s)$ are the voltage and current measurement gain respectively. The system output voltage is 400 V, and its reference voltage u_{ref} is set to 4.0 V, so the voltage sampling factor $H_1(s)$ is kept at 0.01. The current measurement gain $H_2(s)$ is kept at 0.1.

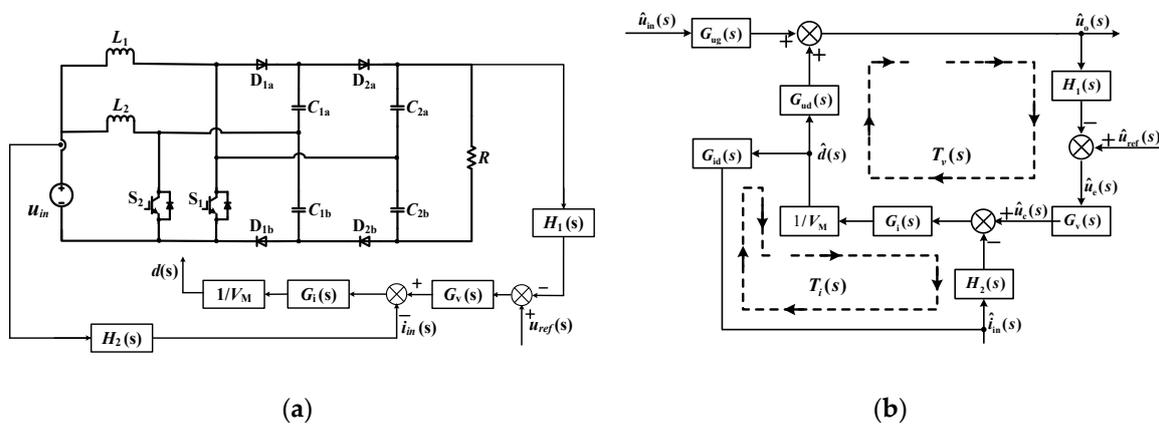


Figure 10. Voltage control system: (a) for converter circuit with 2 VMs; (b) control schematic diagram.

The voltage loop gain is affected by the current loop gain, so the design of the current loop compensator needs to be completed first. The current loop gain without the current loop compensator $G_i(s)$ can be obtained by (18) as $T_{i-e}(s)$.

$$T_{i-e}(s) = G_{id}(s) \cdot \frac{1}{V_M} \cdot H_2(s) \tag{18}$$

Based on Table 3 and (18) and the above parameters of V_M and $H_2(s)$, $G_{id}(s)$ and $T_{i-e}(s)$ can be obtained as follows.

$$G_{id}(s) = \frac{s \cdot 4 + 3200}{s^2 \cdot 6.4 \times 10^{-6} + s \cdot 2.56 \times 10^{-3} + 64} \tag{19}$$

$$T_{i-e}(s) = \frac{s \cdot 0.4 + 320}{s^2 \cdot 8.512 \times 10^{-6} + s \cdot 3.405 \times 10^{-3} + 85.12} \quad (20)$$

The current loop compensator $G_i(s)$ with crossover frequency at 4.7 kHz, are designed as in (21). The Bode diagram for current loop gains with and without compensation are shown in Figure 11.

$$G_i(s) = 0.6 \cdot \frac{s + 2500\pi}{s} \quad (21)$$

The voltage loop gain without the voltage loop compensator $G_v(s)$ can be obtained by (22) as $T_{v-e}(s)$.

$$T_{v-e}(s) = \frac{G_i(s) \cdot \frac{1}{V_M} \cdot G_{ud}(s) \cdot H_1(s)}{1 + G_{id}(s) \cdot \frac{1}{V_M} \cdot H_2(s) \cdot G_i(s)} \quad (22)$$

Based on Table 3, (9)–(11), (13), and V_M , $H_1(s)$ and $H_2(s)$, transfer functions $G_{ud}(s)$ and $T_{v-e}(s)$ can be derived as follows.

$$G_{ud}(s) = \frac{-s \cdot 2.56 + 64000}{s^2 \cdot 6.4 \times 10^{-6} + s \cdot 2.56 \times 10^{-3} + 64} \quad (23)$$

$$T_{v-e}(s) = \frac{-s^4 \cdot 1.307 \times 10^{-7} + s^3 \cdot 2.189 \times 10^{-3} + s^2 \cdot 25.26 + s \cdot 3.269 \times 10^4 + 2.567 \times 10^8}{s^5 \cdot 7.245 \times 10^{-11} + s^4 \cdot 2.101 \times 10^{-6} + s^3 \cdot 1.996 \times 10^{-2} + s^2 \cdot 40.92 + s \cdot 1.892 \times 10^5 + 1.284 \times 10^8} \quad (24)$$

The voltage loop compensator $G_v(s)$ with crossover frequency at 513 Hz, are designed as in (25). The Bode diagrams for voltage loop gains with and without compensation are shown in Figure 12.

$$G_v(s) = 2 \cdot \frac{s + 250\pi}{s} \quad (25)$$

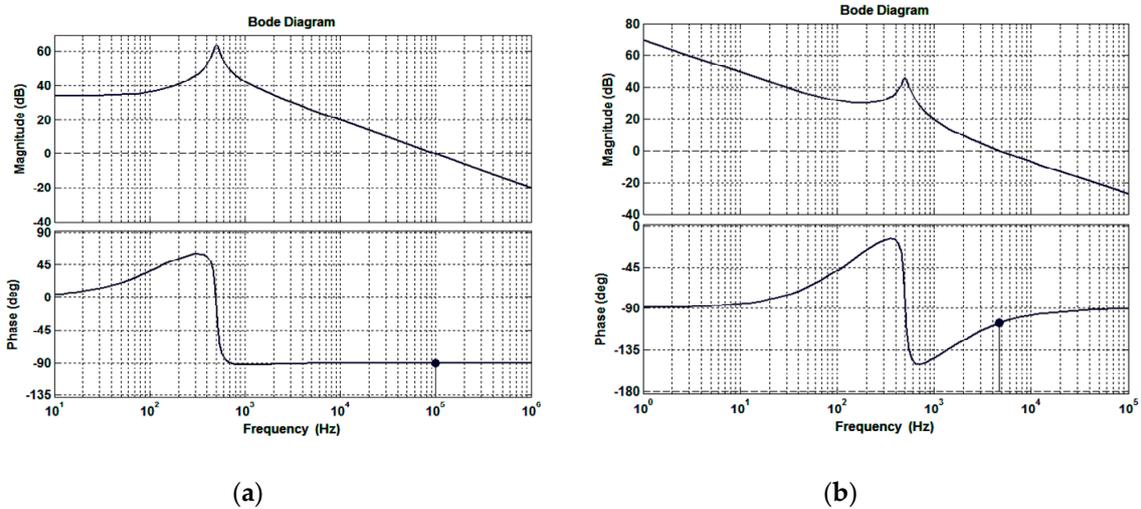


Figure 11. Frequency characteristic of the current loop gain: (a) without compensation (b) with compensation.

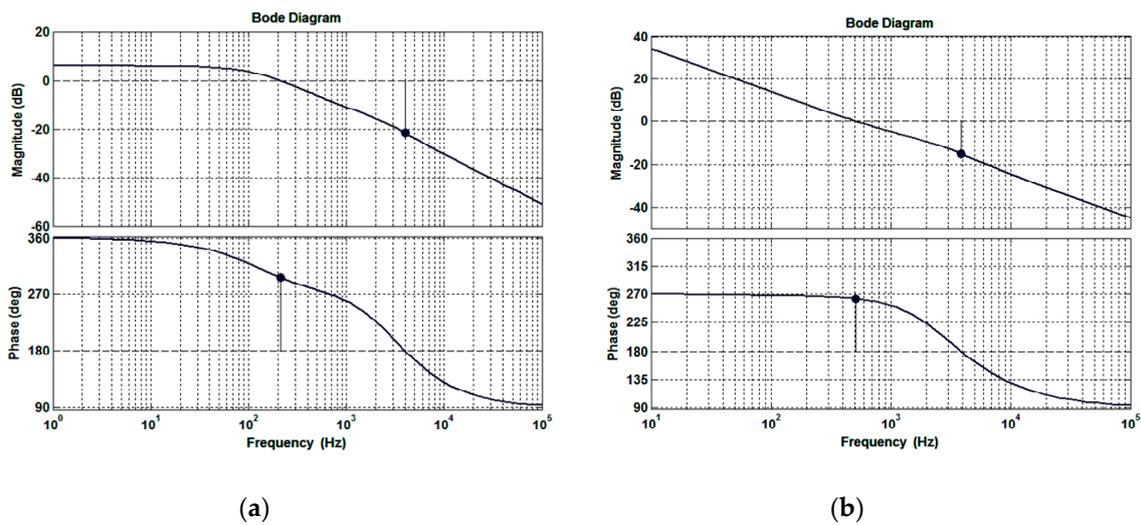


Figure 12. Frequency characteristic of the voltage loop gain (a) without compensation; (b) with compensation.

Furthermore, in order to validate the derived transfer functions (13) and (15) in frequency domain, Bode diagrams for $G_{id}(s)$ and $G_{ud}(s)$ are obtained using both the derived small-signal AC model transfer functions using MATLAB/Simulink, and the computer simulations based on PSIM circuit, as shown in Figure 13. Apparently, the frequency response of the transfer functions from the proposed reduced-order model are in close agreement with the PSIM simulation results within the frequency range below 3 kHz, which means the proposed reduced-order model and the transfer functions can be used in the controller design.

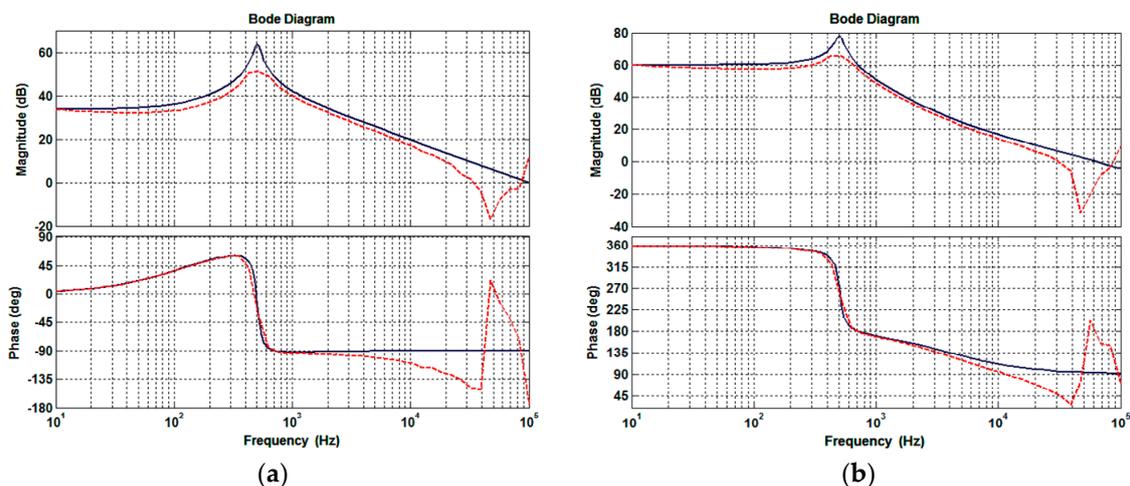


Figure 13. Comparison of frequency responses of the proposed model (black solid lines) and detailed circuit model (red dashed lines): (a) Bode diagram of $G_{id}(s)$; (b) Bode diagram of $G_{ud}(s)$.

5. Simulation and Experimental Verification

This section examines the performance of the controller designed using the method presented in Section 4. The simulation circuit shown in Figure 10a is implemented in PSIM and the simulation results are shown in Figure 14. The specifications of the simulation is given in Table 3 as the rated parameters. Figure 14a shows the response of the output voltage u_o to step changes in the input voltage u_{in} . The input voltage u_{in} increases from 30 V to 40 V, and then drops back to 30 V in 50 ms. Figure 14b shows the simulation waveforms of the output voltage u_o and the output current i_o for step changes in load resistance. The load resistance increases from 400 Ω to 800 Ω first, and then reduces to 400 Ω in

50 ms. Clearly, when u_{in} changes suddenly, u_o is capable of tracking its reference at a constant value, although a small overshoot about 18 V is observed during the transient. When the load resistance suddenly changes, u_o can also follow its reference with a small overshoot of 28 V. It is worth noting that the output voltage will be rapidly re-stabilized to 400 V.

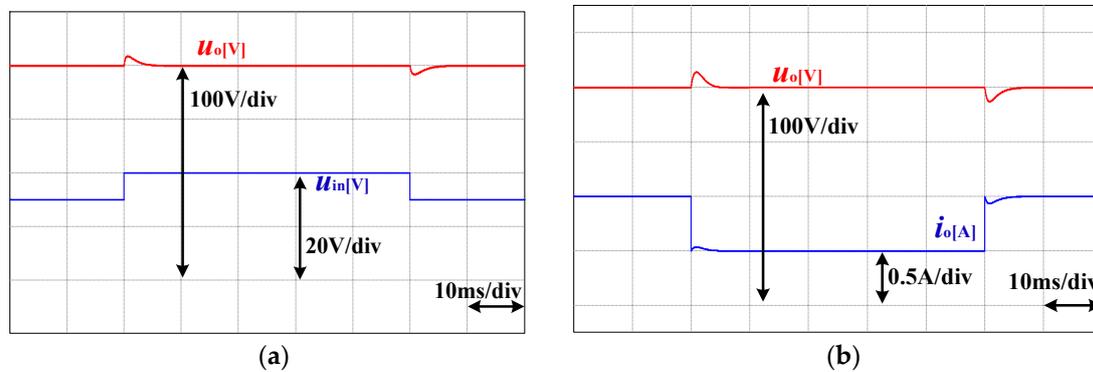


Figure 14. Simulation waveforms for (a) step changes of input voltage; (b) step changes of load resistance.

In order to further verify the efficacy of the proposed model, experimental prototype was set up as shown in Figure 15. The specifications of the experimental prototype are consistent with the rated parameters of the simulation model, as shown in Table 3.

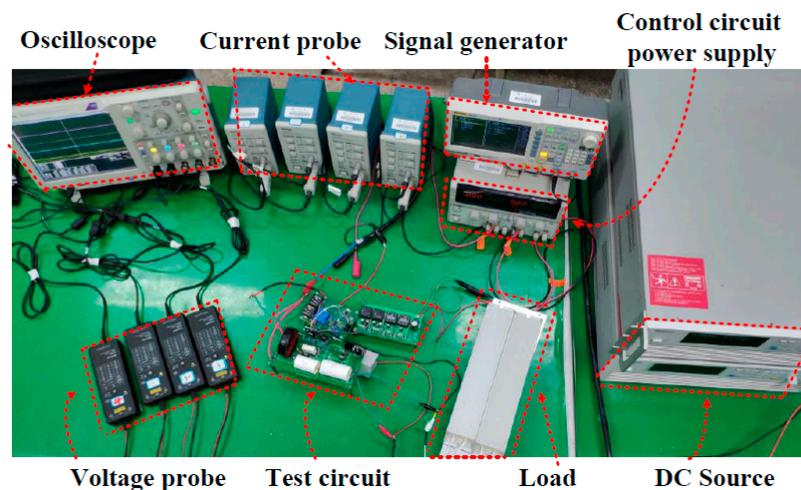


Figure 15. Hardware experimental prototype.

Two scenarios are tested and the experimental results are compared with the simulated results.

First, the input voltage u_{in} increases from 30 V to 40 V and then drops back to 30 V, and the voltage changes are limited by a maximum ramp rate of ± 1 V/ms. The second scenario is similar to that for Figure 14b: the load increases suddenly from 400 Ω to 800 Ω and then drops back to 400 Ω . The experimental waveforms of the circuit variables are shown in Figure 16. It can be clearly observed that in both scenarios, the output voltages are well-regulated at the set-point. The overshoot of the output voltage is much smaller than that which is obtained from the simulation shown in Figure 14; such differences are caused by the limitation of the maximum change rate of the of the DC source and the load.

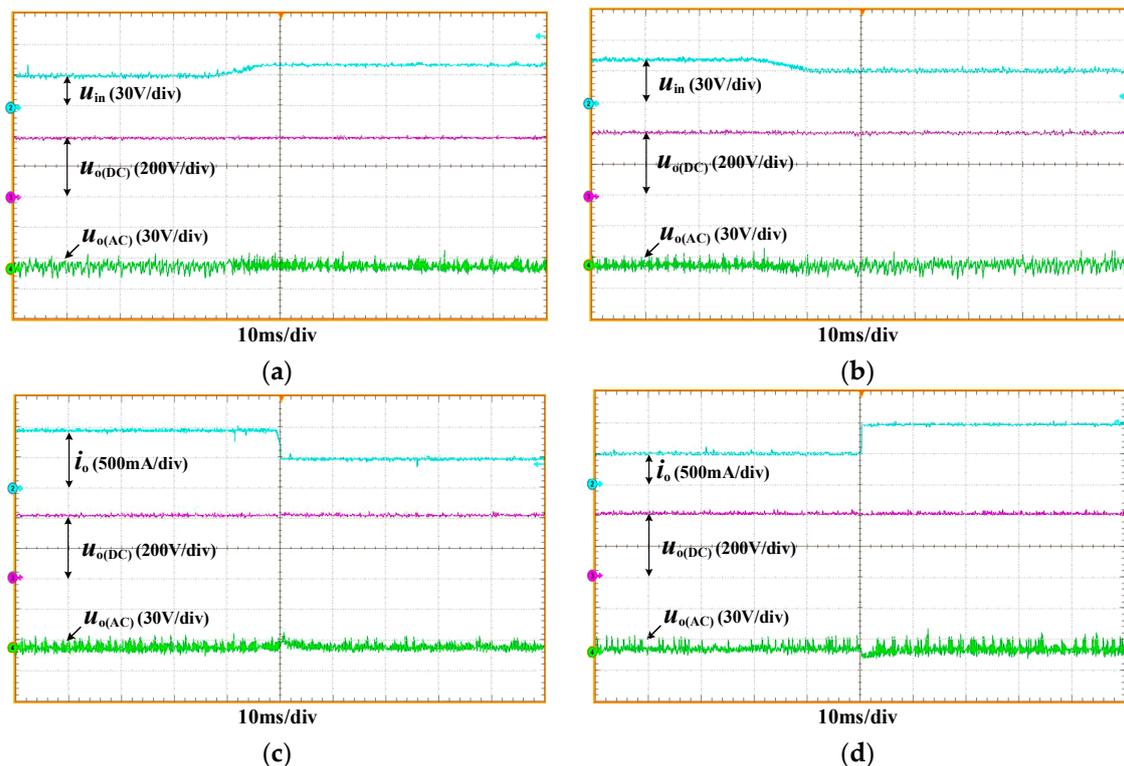


Figure 16. Experimental waveforms of (a) input voltage increases from 30 V to 40 V with ramp rate of 1 V/ms; (b) input voltage decreases from 40 V to 30 V with ramp rate of -1 V/ms; (c) load resistance increases from 400Ω to 800Ω ; (d) load resistance reduces from 800Ω to 400Ω .

6. Conclusions

This paper proposes a method to develop control-oriented reduced-order models for a family of high step-up DC/DC converters based on VM with diode-capacitor network. It was found that a general reduced-order averaged model can be derived by replacing the VM capacitors with output-voltage-controlled sources and performing state-space averaging, and that the simplified model is the same as that of the traditional booster converter with an ideal step-up transformer. The corresponding small-signal AC models and transfer functions have been derived. The proposed approach can be readily applied to other high-gain DC/DC converters circuit using VM, and the model difference only lies in the expressions of circuit parameters of the generic model. Theoretical analysis, simulation and experimental results are given, showing that: (1) the complexity of modeling the high step-up DC/DC converter based on VM can be greatly reduced; (2) the reduced-order model can represent the low-frequency performance of the converter well and it is suitable for control system design.

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