IET Power Electronics

Research Article

Non-isolated high-voltage gain dual-input DC/DC converter with a ZVT auxiliary circuit

Received on 26th May 2018
Revised 8th December 2018
Accepted on 13th December 2018
doi: 10.1049/iet-pel.2018.5465

Binxin Zhu[1] ✉, Qingdian Zeng[1], Don Mahinda Vilathgamuwa[2], Yang Li[2], Xiaoli She[1]

[1]College of Electrical Engineering and New Energy, China Three Gorges University, Yichang, People's Republic of China
[2]School of Electrical Engineering and Computer Science, Queensland University of Technology, Brisbane, Australia
✉ *E-mail: zhubinxin40@163.com*

Abstract: A non-isolated high-voltage gain dual-input DC/DC converter with a zero voltage turn-off (ZVT) auxiliary circuit has been presented. Two photovoltaic (PV) modules can be connected to the proposed converter with separate maximum power point tracking (MPPT). The cost of whole PV power generation system can be decreased significantly as a single converter is employed instead of two converters. All switches can achieve ZVT by an auxiliary circuit, and turn-off switching losses can be decreased and the efficiency of the converter can be improved. Working principle and performance characteristics of the proposed converter are analysed in detail, a dual-input maximum power point tracking control algorithm has been designed for the proposed converter. An 800 W experimental prototype has been built to verify the theoretical analysis.

1 Introduction

Each photovoltaic (PV) module needs a traditional single-input high step-up DC/DC converter to boost its lower output voltage to a higher voltage for the inverter or DC bus as shown in Fig. 1 [1–3]. If many PV panels can be connected to one multi-input converter together, as shown in Fig. 2, not only the system structure can be simplified but also the system cost can be reduced [4–6]. Thus, in recent years, numerous multi-input DC/DC converters have been proposed and well received [7–21].

Isolated converters can use a multi-winding transformer to construct a variety of multi-input DC/DC converters, the voltage gain can also be further improved by changing the turn ratio of the transformer [7–10]. However, the design of multi-winding transformer with a larger turn ratio is difficult and the input current ripple of such converters is large which makes it not suitable for PV power generation [11].

Some non-isolated multiple input DC/DC converters have been realised by inserting a switch between the power source and the input terminal of the traditional DC/DC converter [12–15]. The topology of these multi-input converters is simple and is of low cost. However, only one power source can supply power to the load at one time. Some double- or multiple-input DC/DC converters have been constructed by connecting a number of conventional converters in series, and all power sources can supply power simultaneously [11, 16]. Nevertheless, there are too many semiconductor devices on the current conduction path and that leads to large conduction losses. Moreover, the structure of this kind of converter is complex and the cost is also high. A dual-input high step-up DC/DC converter based on coupled inductors has been proposed in [17]; it can transfer the input power from one port to another input port, which makes it suitable for the power generation system with energy storage units. Bridge-type dual-input DC/DC converter topologies are introduced in [18], and both power sources in these converters have the capability in delivering power to the load simultaneously. However, these converters are not suitable for the PV power generation system due to the limited voltage conversion ratio. Three kinds of high step-up dual-input DC/DC converters have been proposed based on different types of voltage multiplier (VM) circuits in [19–21]. These converters have some advantages such as lower voltage stress on semiconductor components; all power supplies can provide energy at the same time and lower input current ripple, which make them suitable for the PV power generation system. However, the conversion efficiency of these converters is relatively low due to hard switching.

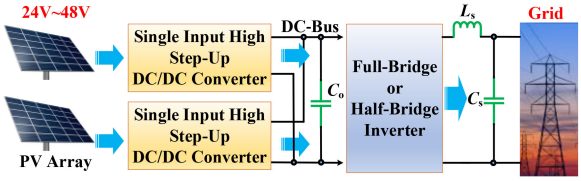

Fig. 1 *PV power generation system with the traditional single-input converter*

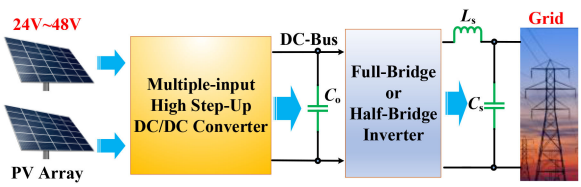

Fig. 2 *PV power generation system structure with the multiple-input converter*

With the proposed zero voltage turn-off (ZVT) circuit and dual-input maximum power point tracking (DMPPT) algorithm for the non-isolated high-voltage gain dual-input ZVT DC/DC converter presented in [22], the power conversion efficiency of the converter is significantly improved. The performance analysis of the proposed converter is discussed in Section 2, experimental results of ZVT are presented in Section 3, and the DMPPT algorithm is discussed and tested in Section 4. The results show that two PV panels can work on MPP simultaneously with the proposed converter and that energy harvested can be delivered to the load efficiently.

2 Performance analysis

2.1 Operation principles

Fig. 3 illustrates the topology of the proposed converter. V_{in1} and V_{in2} denote the two input voltage sources, C_{a1}, C_{a2}, D_{a1}, D_{a2}, D_{a3}, and D_{a4} constitute the ZVT auxiliary circuit for the switches S_1 and S_2. C_1, C_2, D_1 and D_2 constitute the first VM, C_{n1}, C_{n2} and D_{n1}, D_{n2} constitute the nth VM. The number of VMs can be adjusted according to the needs of application.

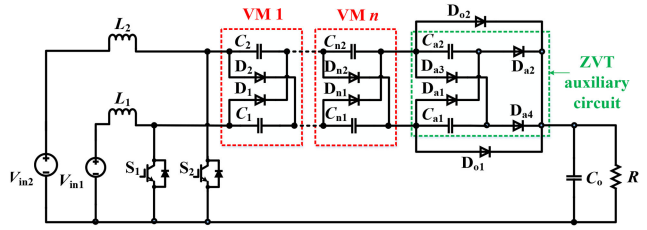

Fig. 3 *Topology of the proposed dual-input DC/DC converter with n VMs*

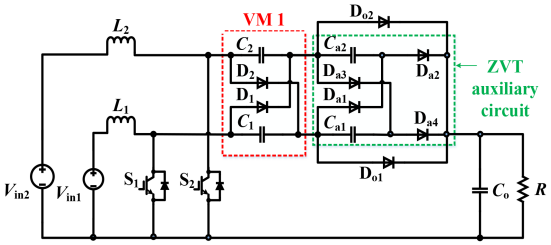

Fig. 4 *Topology of the proposed dual-input DC/DC converter with 1 VM*

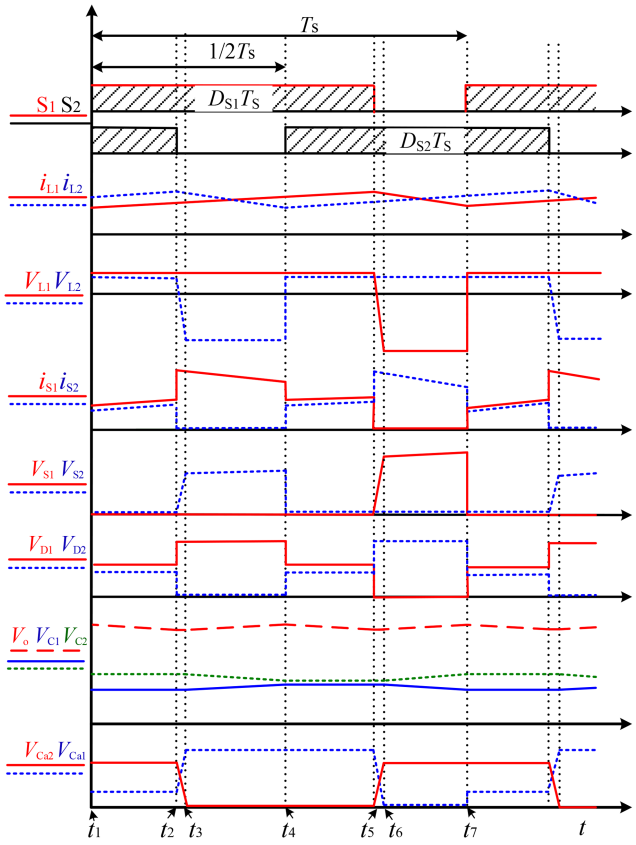

Fig. 5 *Key waveforms of the proposed converter during one switch period*

To facilitate the analysis, the operation principle of the proposed converter has been analysed with 1 VM, as shown in Fig. 4. Also, some assumptions have been made as follows:

i. The inductances of L_1 and L_2 are equal and working on the continuous conduction mode.
ii. All devices are ideal and the effects of parasitic parameters are ignored.
iii. The capacitances of C_1, C_2, and C_o are assumed to be large enough; then the voltage ripple of them can be ignored. Also, the voltage of the capacitor C_2 is higher than the voltage of the capacitor C_1.
iv. The control the signal of the switch S_1, S_2 are interleaved with 180°, and D_{S1} and D_{S2} denote the duty ratio of the switches, respectively, and both of them are >0.5.

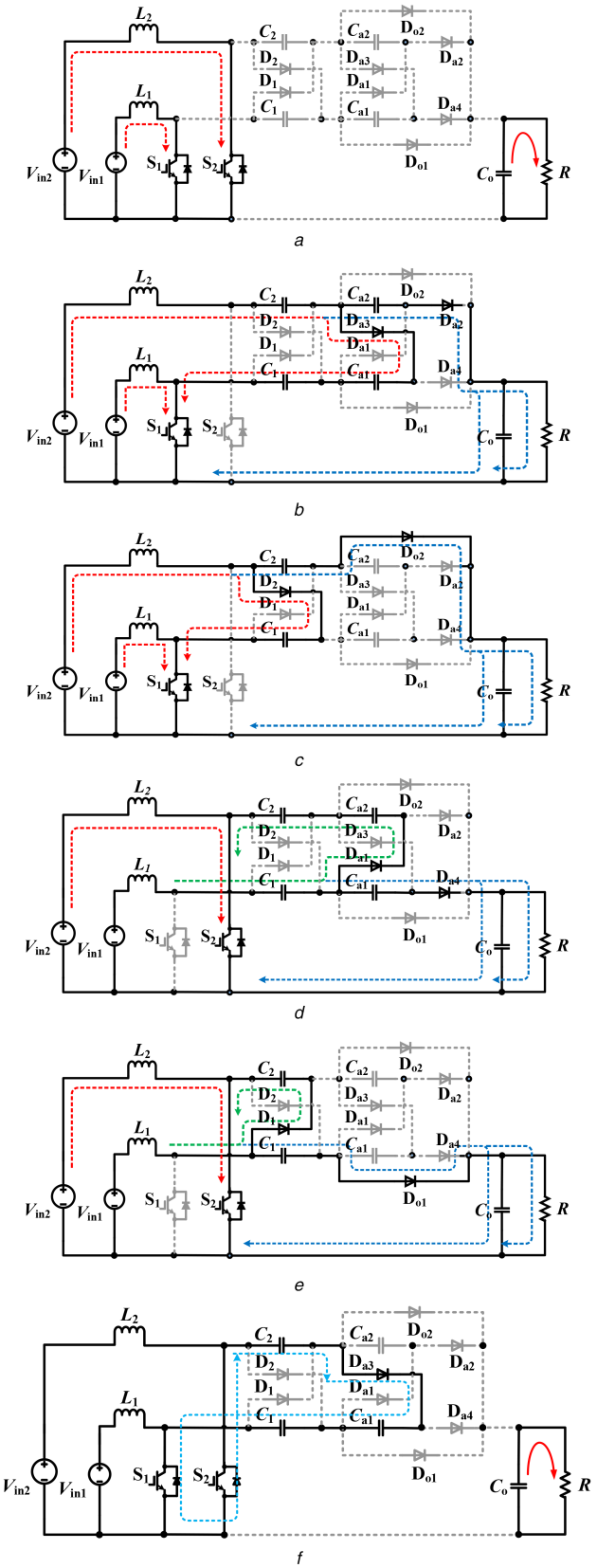

Fig. 6 *Equivalent circuits of the proposed converter*
(a) Mode 1, 4 [t_1–t_2, t_4–t_5], ***(b)*** Mode 2 [t_2–t_3], ***(c)*** Mode 3 [t_3–t_4], ***(d)*** Mode 5 [t_5–t_6], ***(e)*** Mode 6 [t_6–t_7], ***(f)*** Mode 7 [t_7]

According to the working state of the switches, the operation mode of the converter can be separated into seven distinct modes during one switching period T_S as shown in Fig. 5, and its corresponding equivalent circuits are shown in Fig. 6.

Modes 1 and 4 [t_1–t_2, t_4–t_5]: Switches S_1 and S_2 are turned on. During this stage, the two input voltage sources charge the

inductors L_1 and L_2, respectively. Both inductor currents are increasing linearly, and the load is supplied by the capacitor C_o; all diodes are turned off.

Mode 2 [t_2–t_3]: Switch S_2 is turned off at t_2. During this stage, D_1, D_2, D_{o1}, D_{o2}, D_{a1}, D_{a4} are all turned off; D_{a2} and D_{a3} are both turned on. Capacitor C_{a1} is charged from V_{C2}–V_{C1} to V_{C2} through V_{in2}, L_2, C_2, D_{a3}, C_1, and S_1, while capacitor C_{a2} is discharged from V_{C1} to 0 through V_{in2}, L_2, C_2, D_{a2}, and C_o. The voltage across S_2 is increased from 0 to V_{C1}, and the rate of change of voltage across S_2 is the same as those across C_{a1} and C_{a2}, which can be adjusted and limited by the capacitances C_{a1} and C_{a2}. This state ends at t_3.

Mode 3 [t_3–t_4]: During this stage, S_1 is turned on and S_2 is turned off, D_1, D_{o1}, D_{a1}, D_{a2}, D_{a3}, and D_{a4} are all turned off; both D_2 D_{o2} are turned on. Part of the current of the inductor L_2 flows through L_2, C_2, D_{o2}, the load, and V_{in2}. The other part flows through L_2, D_2, C_1, S_1, and V_{in2}. In this interval, C_1 and C_o are charged, while C_2 is discharged.

Mode 5 [t_5–t_6]: Switch S_1 is turned off at t_5. During this stage, D_1, D_2, D_{o1}, D_{o2}, D_{a2}, D_{a3} are all turned off; both D_{a1} and D_{a4} are turned on. Capacitor C_{a1} is discharged from V_{C2} to 0 through V_{in1}, L_1, C_1, D_{a4}, and C_o, while capacitor C_{a2} is charged from 0 to V_{C1} through V_{in1}, L_1, D_{a1}, C_2, and S_2. Similar to mode 2, the rate of change of voltage across S_1 can also be adjusted and limited by the capacitances C_{a1} and C_{a2}. This state ends at t_6.

Mode 6 [t_6–t_7]: Switch S_1 is turned off and S_2 is turned on. Diodes D_2, D_{o2}, D_{a1}, D_{a2}, D_{a3}, and D_{a4} are all turned off; both D_1 and D_{o1} are turned on. In this stage, part of the current of the inductor L_1 flows through L_1, C_1, D_{o1}, the load, and V_{in1}. The other part flows through L_1, D_1, C_2, S_2, and V_{in1}. In this interval, C_2 and C_o are charged, while C_1 is discharged.

Mode 7 [t_7]: V_{C1} is determined by V_{in2} and D_{S2}, while V_{C2} is determined by V_{in1} and D_{S1} as shown in (3). As stated in the assumptions earlier that if $V_{C2} > V_{C1}$, when S_1 is turned on, C_2 will discharge to the capacitor C_{a1} through D_{a3}, C_1, S_1, and S_2. C_{a1} will increase from 0 to V_{C2}–V_{C1}. Since the capacitance of C_{a1} is very small compared to C_1 and C_2, both the duration and influence of this mode can be ignored.

2.2 Voltage gain expression

By analysing the steady-state condition of the proposed converter, the volt-second balance can be applied to the inductors L_1 and L_2 (modes 2, 5, and 7 are ignored due to their short occurrence time in one switching cycle). Equations (1) and (2) can be obtained from modes 1, 3, 4, and 6 (as shown in Figs. 6(a), (c) and (e)):

$$\begin{cases} (V_{C2} - V_{in1})(1 - D_{S1}) = V_{in1} D_{S1} \\ (V_{Co} - V_{C1} - V_{in1})(1 - D_{S1}) = V_{in1} D_{S1} \end{cases} \tag{1}$$

$$\begin{cases} (V_{C1} - V_{in2})(1 - D_{S2}) = V_{in2} D_{S2} \\ (V_{Co} - V_{C2} - V_{in2})(1 - D_{S2}) = V_{in2} D_{S2} \end{cases} \tag{2}$$

Then, it can be concluded from (1) and (2) that

$$\begin{cases} V_{C1} = \dfrac{V_{in2}}{1 - D_{S2}} \\ V_{C2} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_o = V_{Co} = \dfrac{V_{in1}}{1 - D_{S1}} + \dfrac{V_{in2}}{1 - D_{S2}} \end{cases} \tag{3}$$

The same can be obtained with n VMs; the output voltage can be expressed as

$$V_o = \frac{n+1}{2}\left(\frac{V_{in2}}{1 - D_{S2}} + \frac{V_{in1}}{1 - D_{S1}}\right), \quad \text{where } n = 1, 3, 5, 7\ldots \tag{4}$$

2.3 Voltage stress of semiconductor devices

To simplify the analysis process, the voltage ripples of the capacitors are ignored. The voltage stress across switches S_1 and S_2 can be expressed as follows:

$$\begin{cases} V_{S1} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_{S2} = \dfrac{V_{in2}}{1 - D_{S2}} \end{cases} \tag{5}$$

The voltage stresses of the output diodes D_{o1} and D_{o2} are V_{Do1} and V_{Do2}, respectively, and the voltage stresses of the diodes D_1 and D_2 in the VM are V_{Do1} and V_{Do2}, respectively,

$$\begin{cases} V_{Do1} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_{Do2} = \dfrac{V_{in2}}{1 - D_{S2}} \\ V_{D1} = V_{D2} = \dfrac{V_{in2}}{1 - D_{S2}} + \dfrac{V_{in1}}{1 - D_{S1}} \end{cases} \tag{6}$$

The diode voltage stresses in the ZVT auxiliary circuit are

$$\begin{cases} V_{Da1} = V_{Da2} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_{Da3} = V_{Da4} = \dfrac{V_{in2}}{1 - D_{S2}} \end{cases} \tag{7}$$

The analysis of the converter with n VMs is carried out in this paper, and the voltage stress of the switch and the diode can be obtained as follows:

$$\begin{cases} V_{S1} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_{S2} = \dfrac{V_{in2}}{1 - D_{S2}} \end{cases} \tag{8}$$

$$\begin{cases} V_{Do1} = \dfrac{V_{in1}}{1 - D_{S1}} \\ V_{Do2} = \dfrac{V_{in2}}{1 - D_{S2}} \\ V_{D1} = V_{D2} = \cdots = V_{Dn1} = V_{Dn2} = \dfrac{V_{in2}}{1 - D_{S2}} + \dfrac{V_{in1}}{1 - D_{S1}} \end{cases} \tag{9}$$

2.4 Relationship of the two input currents and the current stress of semiconductor devices

The average values of the inductor currents i_{L1} and i_{L2} are denoted as I_{L1} and I_{L2}, respectively. The average current of D_1, D_2, D_{o1}, D_{o2}, S_1, and S_2, are denoted as I_{D1}, I_{D2}, I_{Do1}, I_{Do2}, I_{S1}, and I_{S2}, respectively. Ampere-second balance can be applied to the capacitors C_1 and C_2 as

$$I_{L2}(1 - D_{S2})T_S = I_{L1}(1 - D_{S1})T_S \tag{10}$$

The current relationship of the two input currents is as follows:

$$I_{L2}(1 - D_{S2}) = I_{L1}(1 - D_{S1}) \tag{11}$$

Equation (11) shows that by controlling the duty cycle of the switches S_1 and S_2, the two input currents can be controlled to achieve the MPPT. The same conclusion can be obtained when the converter consists of n VMs.

Table 1 Comparison with other structures

Topology	Proposed converter	Converter in [19]	Converter in [20]	Converter in [21]
number of switches	2	2	2	2
number of diodes	$2 + 2n + 4$(ZVT)	4	$1 + 2n$	$1 + n$
voltage stress on switches	$\frac{u_{in}}{1-D}$	$\frac{u_{in}}{1-D}$	$\frac{u_{in}}{1-D}$	$\frac{u_{in}}{1-D}$
voltage stress on diodes	$\frac{u_{in}}{1-D}$	$\frac{2u_{in}}{1-D}$	$\frac{2u_{in}}{1-D}$	$\frac{2u_{in}}{1-D}$
voltage conversion ratio	$\frac{1+n}{1-D}$	$\frac{4}{1-D}$	$\frac{1+2n}{1-D}$	$\frac{1+n}{1-D}$
ZVT	yes	no	no	no
adjust voltage conversion ratio	yes	no	yes	yes

Table 2 Parameters of experimental prototype

Component	Model/value
S_1, S_2	IKW75N65EL5
D_1, D_2, D_{o1}, D_{o2}, D_{a1}, D_{a2}, D_{a3}, D_{a4}	IDT12S60C
C_1, C_2	10 μF
C_o	20 μF
C_{a1}, C_{a2}	20 nF
L_1, L_2	320 μH
switch frequency	50 kHz
input voltage (V_{in1}/V_{in2})	45 V/40 V
duty cycle (D_{S1}/D_{S2})	80%/77.1%
load resistor (R)	200 Ω
output voltage	400 V
output power	800 W

The average value of the output current is I_o; (12) can be obtained according to the ampere-second balance of the capacitor C_o:

$$I_o = I_{Do1} + I_{Do2} \tag{12}$$

When the capacitance of C_1 is equal to C_2, the average current of diodes can be expressed as (13). The similar conclusion can be obtained as (14) when the converter consists of n VMs:

$$I_{D1} = I_{D2} = I_{Do1} = I_{Do2} = \frac{I_o}{2} \tag{13}$$

$$I_{D1} = I_{D2} = \cdots = I_{Dn1} = I_{Dn2} = I_{Do1} = I_{Do2} = \frac{I_o}{2} \tag{14}$$

The average current of the switches S_1 and S_2 are denoted as I_{S1} and I_{S2}, respectively,

$$\begin{cases} I_{S1} = I_{L1} \cdot D_{S1} + \dfrac{I_{L2} \cdot (1 - D_{S2})}{2} \\ I_{S2} = I_{L2} \cdot D_{S2} + \dfrac{I_{L1} \cdot (1 - D_{S1})}{2} \end{cases} \tag{15}$$

2.5 Design of the capacitors in the ZVT auxiliary circuit

Two factors need to be considered when optimising the design of the capacitor value. First, the values of C_{a1} and C_{a2} should be as small as possible to minimise their impact on the performance of the converter. Second, the values of C_{a1} and C_{a2} also should be large enough to achieve ZVT of the switches. In order to achieve the above goals, the following two design criteria are used in this paper.

1. In order to limit the change of converter performance due to the ZVT circuit, the time of modes 2 and 5 should be <5% of the whole switching period (the time of modes 2 and 5 correspond to the rise time of the terminal voltage of S_1 and S_2, respectively, defined as $\Delta t_{rise\text{-}time}$).

$$\Delta t_{rise-time} \le 0.05 \cdot T_S \tag{16}$$

2. In order to ensure the effect of ZVT, the voltage rise time $\Delta t_{rise\text{-}time}$ of the switches should be large enough than the turn-off time of the IGBT (the turn-off time t_{off} can be obtained from the datasheet). Also, $\Delta t_{rise\text{-}time}$ is designed to >3 times of the t_{off} in this paper:

$$\Delta t_{rise-time} \ge 3t_{off} \tag{17}$$

From mode 5, when S_1 is turned off, C_{a1} is discharged from V_{C2} to 0, while C_{a2} is charged from 0 to V_{C1}, (24) can be obtained. Similarly, (25) can be obtained from mode 2:

$$C_{a1} \cdot V_{C2} + C_{a2} \cdot V_{C1} = I_{L1} \cdot \Delta t_{rise-time1} \tag{18}$$

$$C_{a1} \cdot V_{C1} + C_{a2} \cdot V_{C1} = I_{L2} \cdot \Delta t_{rise-time2} \tag{19}$$

To simplify the design process, the values of C_{a1} and C_{a2} can be set equal as C_a, and then (26) can be obtained. $\Delta t_{rise\text{-}time1}$, $\Delta t_{rise\text{-}time2}$ means the time of modes 5 and 2, respectively,

$$\begin{cases} \Delta t_{rise-time1} = \dfrac{C_a \cdot (V_{C2} + V_{C1})}{I_{L1}} \\ \Delta t_{rise-time2} = \dfrac{2C_a \cdot V_{C1}}{I_{L2}} \end{cases} \tag{20}$$

Apparently, substituting (20) into (16) and (17), the capacitors of C_{a1} and C_{a2} could be designed.

2.6 Comparison with other structures

Numerous VM circuits have been developed and combined with the conventional boost converter to achieve many dual-input high step-up DC/DC converter topologies as given in [19–21]. Performance comparison among these converters and the proposed converter is given in Table 1. If the voltage conversion ratio is set to be equal, the number of switches of the proposed converter is same as that of the other converters presented in Table 1, and the number of diodes of the proposed converter is larger than that of others. However, not only the voltage stress on diodes of the proposed converter is lower than other structures, but also ZVT has been achieved.

3 Experimental verification

In order to validate the above theoretical analysis, an 800 W experimental prototype has been designed; the parameters of the prototype are shown in Table 2.

Fig. 7*a* shows the waveforms of i_{L1}, i_{L2}, V_{gs1}, and V_{gs2}. The output voltage V_o is equal to 400 V from the measured results in Fig. 7*b* which is consistent with the theoretical calculation. Fig. 7*c* contains the waveforms of V_{C1}, V_{C2}, V_{Ca1}, and V_{Ca2}; the measured

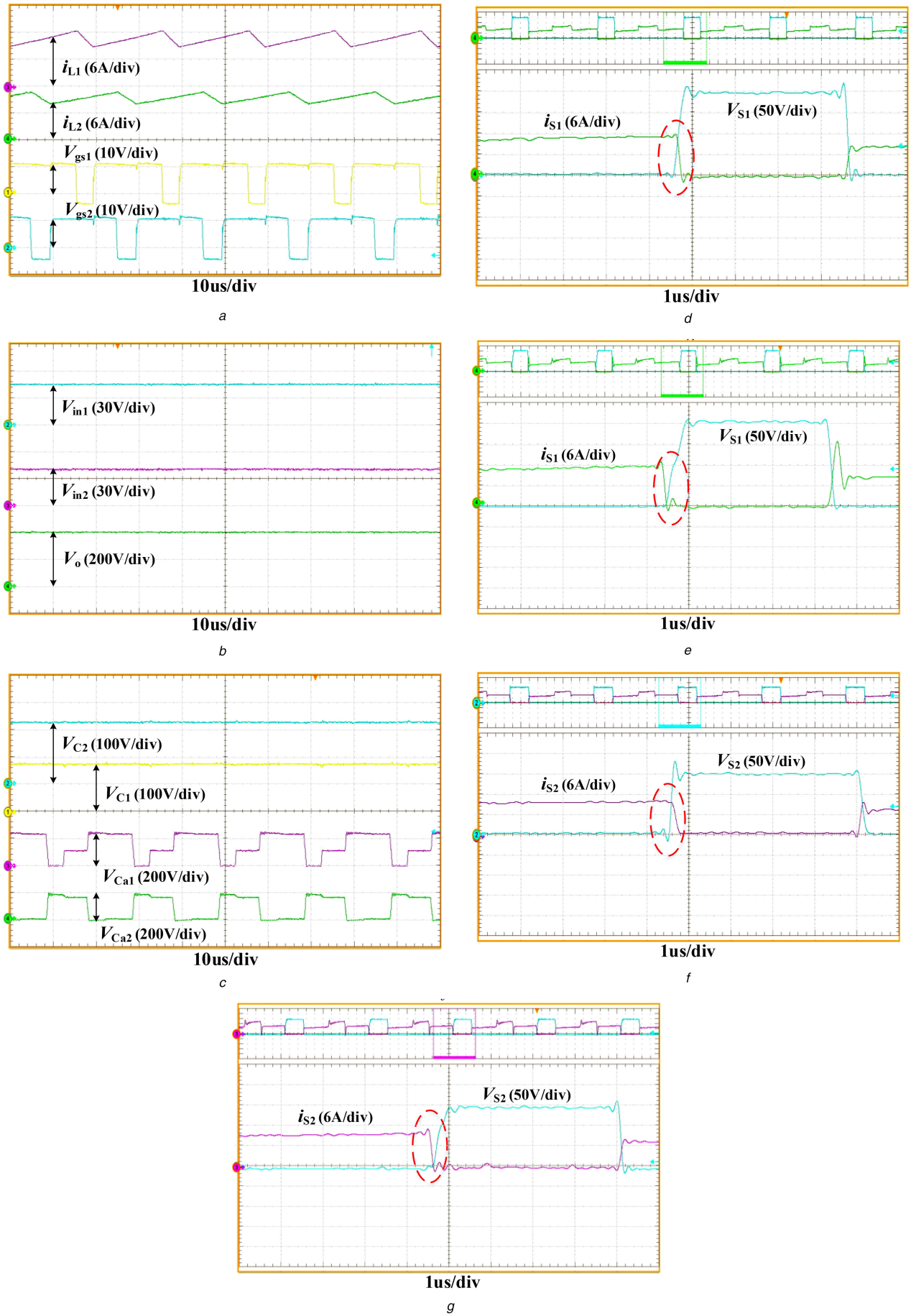

Fig. 7 *Experimental waveforms*

(a) Inductor currents and duty cycles, ***(b)*** Input voltages and output voltage, ***(c)*** V_{C1}, V_{C2}, V_{Ca1}, and V_{Ca2}, ***(d)*** S_1 current and voltage without the ZVT auxiliary circuit, ***(e)*** S_1 current and voltage with the ZVT auxiliary circuit, ***(f)*** S_2 current and voltage without the ZVT auxiliary circuit, ***(g)*** S_2 current and voltage with the ZVT auxiliary circuit

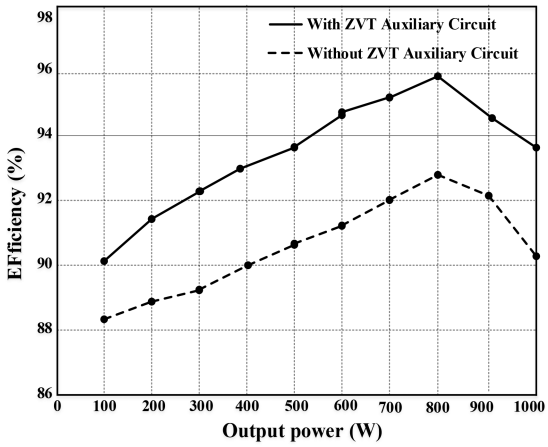

Fig. 8 *Efficiency curve*

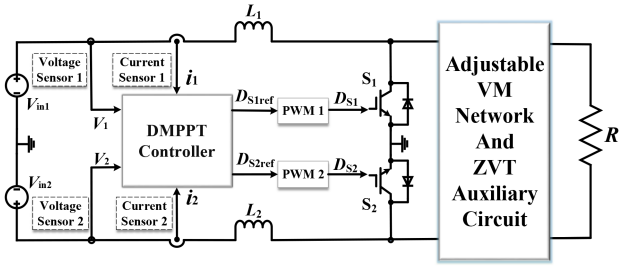

Fig. 9 *Proposed DMPPT control block diagram*

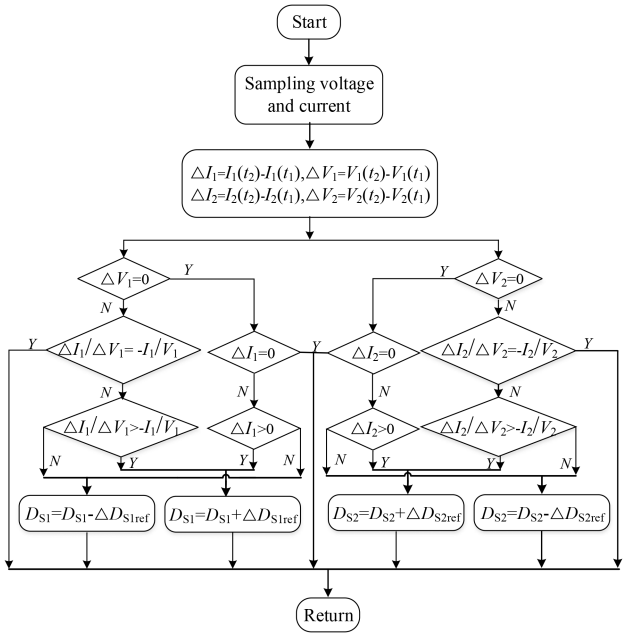

Fig. 10 *Proposed DMPPT control algorithm*

results are all consistent with the theoretical analysis. Figs. 7*d* and *f* show the voltage and current waveforms of S_1 and S_2 when they were turned off without the proposed ZVT auxiliary circuit, and Figs. 7*e* and *g* show their waveforms when S_1 and S_2 were turned off with the proposed ZVT auxiliary circuit. Obviously, with the help of the auxiliary circuit, both switches S_1 and S_2 have achieved ZVT. Therefore, the efficiency of the converter has been significantly improved. Moreover, the oscillations of the voltage waveforms during the switch turn-off process have been effectively mitigated, which will help to reduce the EMI effects of the converter.

Fig. 8 shows the efficiency graph of the proposed converter with and without the proposed ZVT auxiliary circuit at different output power levels. As the output power increases, both efficiency curves reach their respective maximum values around the output power of 800 W, which are recorded as 96 and 93% with and without ZVT, respectively. Within the variation range of the output power, the efficiency of the converter is increased as a result of the proposed ZVT auxiliary circuit.

Table 3 Parameters of PV panel

Parameter	Value
maximum output power	200 W
open circuit voltage (V_{oc})	45.6 V
short current (I_{sc})	5.8 A
the maximum power point voltage (V_m)	36.9 V
the maximum power point current (I_m)	5.42 A

4 Dual-input maximum power point tracking

4.1 DMPPT implementation scheme

DMPPT control strategy of the proposed converter has been designed based on the incremental conductance method. Fig. 9 shows the proposed DMPPT control block diagram. First, the input voltage and current are sampled. Then the input power of two PV panels is determined by multiplying the voltage and current measurements. Finally, depending on the value of the incremental conductance, the required duty ratio is obtained based on the following conditions.

Based on the incremental conductance method [23], (21) can be obtained:

$$\begin{cases} \dfrac{\Delta I}{\Delta V} = -\dfrac{I}{V}, & \text{working on the MPP} \\ \dfrac{\Delta I}{\Delta V} > -\dfrac{I}{V}, & \text{working on the left of MPP} \\ \dfrac{\Delta I}{\Delta V} < -\dfrac{I}{V}, & \text{working on the right of MPP} \end{cases} \tag{21}$$

Obviously, from (21), when $\Delta I/\Delta V$ is equal to $-I/V$, the PV panel works at the MPP. If $\Delta I/\Delta V$ is larger than $-I/V$, the PV panel works on the left of the MPP, and then the duty cycle of the switch needs to be increased. If $\Delta I/\Delta V$ is smaller than $-I/V$, the PV panel works on the right of the MPP, and then the duty cycle of the switch needs to be reduced. The DMPPT algorithm for the proposed converter based on the incremental conductance method has been designed as shown in Fig. 10.

4.2 DMPPT experimental results

The PV panels used in the experiment were Lvchen-M200; Table 3 shows its rated parameters.

It is important to detect the maximum power of the PV panel under the environmental radiation and temperature conditions, which can provide a reference to verify whether the MPP is achieved by the proposed DMPPT control strategy. By changing the load resistance value, the output power of the PV panel can be obtained by multiplying the output voltage and current of the PV panel. The experimental results are shown in Fig. 11.

Under the environmental conditions during the test, the maximum power of the PV panel is recorded ~77 W from the measured results in Fig. 11. DMPPT experiment results of the PV panels 1and 2 are illustrated in Fig. 12. Before changing the radiation intensity, both PV panels 1 and 2 work at the MPP. At t = 6 s, the radiation intensity of the PV panel 1 is reduced by using a coloured glass, as can be observed from the results that the output power drops rapidly. At t = 10 s, the coloured glass has been moved, and then the PV panel 1 returns to the MPP immediately. The PV panel 2 shows similar results. Apparently, the above results show that the proposed DMPPT control strategy is effective and the whole system can track the MPP quickly when the radiation intensity changes.

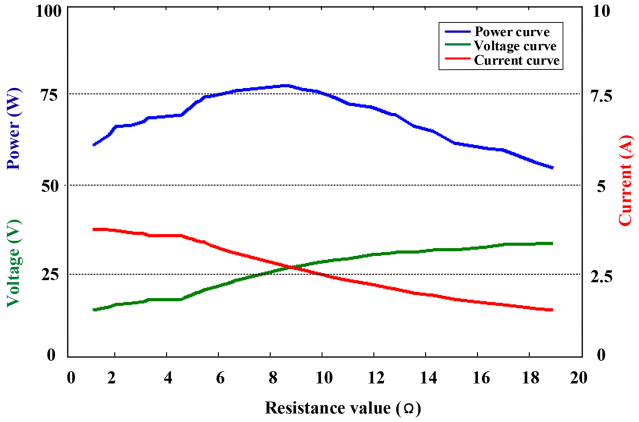

Fig. 11 *Output power, voltage, and current of the PV panel*

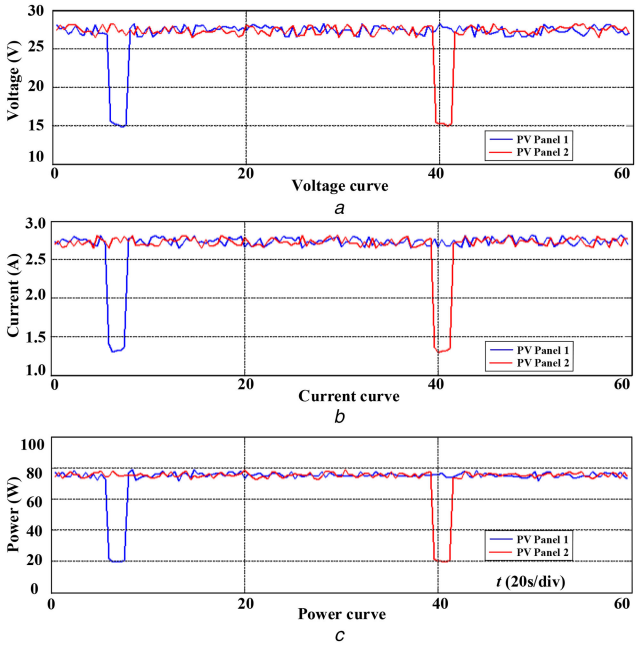

Fig. 12 *Output voltage, current, and power curve of panels 1 and 2*

5 Conclusion

A ZVT non-isolated high-voltage gain dual-input DC/DC converter with the corresponding DMPPT control algorithm has been proposed in this paper for PV power generation. Theoretical analysis and experimental results show that the efficiency of the converter can be improved by the proposed ZVT auxiliary circuit; at the same time, two PV panels can be connected to the proposed converter together, and both of them can track MPP simultaneously. Apparently, not only the cost of the PV power generation system can be reduced, but also the conversion efficiency of the converter can be improved by the proposed circuit.

6 Acknowledgment

This project was supported by the National Natural Science Foundation of China (51707103).

7 References

[1] Li, W., He, X.: 'Review of nonisolated high-step-up dc/dc converters inphotovoltaic grid-connected applications', *IEEE Trans. Ind. Electron.*, 2011, **58**, (4), pp. 1239–1250

[2] Evran, F., Aydemir, M.T.: 'Isolated high step-up dc–dc converter with low voltage stress', *IEEE Trans. Power Electron.*, 2014, **29**, (7), pp. 3591–3603

[3] Liang, T.J., Lee, J.H.: 'Novel high-conversion-ratio high-efficiency isolated bidirectional dc–dc converter', *IEEE Trans. Ind. Electron.*, 2015, **62**, (7), pp. 4492–4503

[4] Chen, Y.M., Liu, Y.C., Lin, S.H.: 'Double-input pwm dc/dc converter for high-/low-voltage sources', *IEEE Trans. Ind. Electron.*, 2006, **53**, (5), pp. 1538–1545

[5] Guo, F., Fu, L., Zhang, X., *et al.*: 'A family of quasi-switched-capacitor circuit-based dual-input dc/dc converters for photovoltaic systems integrated with battery energy storage', *IEEE Trans. Power Electron.*, 2016, **31**, (12), pp. 8237–8246

[6] Ajami, A., Asadi Shayan, P.: 'Soft switching method for multiport dc/dc converters applicable in grid connected clean energy sources', *IET Power Electron.*, 2015, **8**, (7), pp. 1246–1254

[7] Chen, Y.-M., Liu, Y.-C., Wu, F.-Y.: 'Multi-input dc/dc converter based on the multiwinding transformer for renewable energy applications', *IEEE Trans. Ind. Appl.*, 2002, **38**, (4), pp. 1096–1104

[8] Krishnaswami, H., Mohan, N.: 'Three-port series-resonant dc–dc converter to interface renewable energy sources with bidirectional load and energy storage ports', *IEEE Trans. Power Electron.*, 2009, **24**, (10), pp. 2289–2297

[9] Zhao, C., Round, S.D., Kolar, J.W.: 'An isolated three-port bidirectional dc-dc converter with decoupled power flow management', *IEEE Trans. Power Electron.*, 2008, **23**, (5), pp. 2443–2453

[10] Tao, H., Duarte, J.L., Hendrix, M.A.M.: 'Three-port triple-half-bridge bidirectional converter with zero-voltage switching', *IEEE Trans. Power Electron.*, 2008, **23**, (7), pp. 782–792

[11] Kumar, L., Jain, S.: 'Multiple-input dc/dc converter topology for hybrid energy system', *IET Power Electron.*, 2013, **6**, (8), pp. 1483–1501

[12] Khaligh, A., Cao, J., Lee, Y.J.: 'A multiple-input dc–dc converter topology', *IEEE Trans. Power Electron.*, 2009, **24**, (3), pp. 862–868

[13] Behjati, H., Davoudi, A.: 'A multiple-input multiple-output dc–dc converter', *IEEE Trans. Ind. Appl.*, 2013, **49**, (3), pp. 1464–1479

[14] Dobbs, B.G., Chapman, P.L.: 'A multiple-input dc-dc converter topology', *IEEE Power Electron. Lett.*, 2003, **1**, (1), pp. 6–9

[15] Babaei, E., Abbasi, O.: 'Structure for multi-input multi-output dc-dc boost converter', *IET Power Electron.*, 2016, **9**, (1), pp. 9–19

[16] Ahmadi, R., Ferdowsi, M.: 'Double-input converters based on h-bridge cells: derivation, small-signal modeling, and power sharing analysis', *IEEE Trans. Circuits Syst. I, Reg. Pap.*, 2012, **59**, (4), pp. 875–888

[17] Wai, R.J., Hong, L.S.: 'High-efficiency dual-input converter with high-voltage gain and internal charge function', *IET Power Electron.*, 2014, **7**, (2), pp. 299–315

[18] Athikkal, S., Kumar, G.G., Sundaramoorthy, K., *et al.*: 'Performance analysis of novel bridge type dual input dc-dc converters', *IEEE. Access.*, 2017, **5**, pp. 15340–15353

[19] Baddipadiga, B.P., Ferdowsi, M.: 'A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier', *IEEE Trans. Power Electron.*, 2017, **32**, (10), pp. 7707–7715

[20] Müller, L., Kimball, J.W.: 'High gain dc–dc converter based on the Cockcroft–Walton multiplier', *IEEE Trans. Power Electron.*, 2016, **31**, (9), pp. 6405–6415

[21] Prabhala, V.A.K., Fajri, P., Gouribhatla, V.S.P., *et al.*: 'A dc–dc converter with high voltage gain and two input boost stages', *IEEE Trans. Power Electron.*, 2016, **31**, (6), pp. 4206–4215

[22] Prudente, M., Pfitscher, L.L., Emmendoerfer, G., *et al.*: 'Voltage multiplier cells applied to non-isolated dc–dc converters', *IEEE Trans. Power Electron.*, 2008, **23**, (2), pp. 871–887

[23] Esram, T., Chapman, P.L.: 'Comparison of photovoltaic array maximum power point tracking techniques', *IEEE Trans. Energy Convers.*, 2007, **22**, (2), pp. 439–449

8 Appendix

The operation principle and the voltage conversion gain of the proposed converter working in DCM have been analysed as follows.

8.1 Operation principle

Compared to CCM, there are two additional operation modes in DCM as shown in Fig. 13. The operation mode of the converter can be separated into nine distinct modes during one switching period T_S as shown in Fig. 14. The two additional operation modes are analysed as follows.

Mode 4 [t_4–t_5]: S_1 is turned on and S_2 is turned off, and at t_4, the inductor current of L_2 is decreased to zero. During this stage, the input voltage sources V_{in1} charge the inductors L_1, the inductor current of L_1 increases linearly, the load is supplied by the capacitor C_o, and all diodes are working in off-state.

Mode 8 [t_8–t_9]: S_2 is turned on and S_1 is turned off, and at t_8, the inductor current of L_1 is decreased to zero. During this stage, the input voltage sources V_{in2} charge the inductors L_2, the inductor current of L_2 increases linearly, the load is supplied by the capacitor C_o, and all diodes are working in off-state.

8.2 Voltage conversion gain

By using the volt-second balance to L_1 and L_2 (modes 2, 6, and 9 are ignored due to their short occurrence time in one switching cycle). The following equations can be deduced:

$$\begin{cases} (V_{C2} - V_{\text{in1}}) \cdot D_{M1} = V_{\text{in1}} D_{\text{S1}} \\ (V_{\text{Co}} - V_{C1} - V_{\text{in1}}) \cdot D_{M1} = V_{\text{in1}} D_{\text{S1}} \end{cases} \tag{22}$$

$$\begin{cases} (V_{C1} - V_{\text{in2}}) \cdot D_{M2} = V_{\text{in2}} D_{\text{S2}} \\ (V_{\text{Co}} - V_{C2} - V_{\text{in2}}) \cdot D_{M2} = V_{\text{in2}} D_{\text{S2}} \end{cases} \tag{23}$$

$$\begin{cases} D_2 = t_8 - t_6 < 1 - D_{\text{S1}} \\ D_3 = t_4 - t_2 < 1 - D_{\text{S2}} \end{cases} \tag{24}$$

Following (22)–(24), (25) can be obtained as

$$\begin{cases} V_{C1} = V_{\text{in2}} \cdot \left(1 + \dfrac{D_{\text{S2}}}{D_{M2}}\right) \\ V_{C2} = V_{\text{in1}} \cdot \left(1 + \dfrac{D_{\text{S1}}}{D_{M1}}\right) \\ V_{\text{Co}} = V_{\text{Co}} = V_{\text{in1}} \cdot \left(1 + \dfrac{D_{\text{S1}}}{D_{M1}}\right) + V_{\text{in2}} \cdot \left(1 + \dfrac{D_{\text{S2}}}{D_{M2}}\right) \end{cases} \tag{25}$$

The duty cycles D_{S1} and D_{S2} are the control signals of the converter and can be considered known. However, D_{M1} and D_{M2} are unknown, and hence the other two equations are needed to eliminate D_{M1} and D_{M2} to get the voltage conversion ratio.

The peak-to-peak current ripple and average current of the inductors L_1 and L_2 can be calculated by (26). Based on the capacitor charge balance of C_1 and C_2, (27) can be obtained. According to the balance of input and output power of the converter, (28) can be deduced:

$$\begin{cases} \Delta i_{L1} = \dfrac{V_{\text{in1}} \cdot D_{\text{S1}} \cdot T_{\text{s}}}{L_1} \\ \Delta i_{L2} = \dfrac{V_{\text{in2}} \cdot D_{\text{S2}} \cdot T_{\text{s}}}{L_2} \\ I_{L1} = \dfrac{\Delta i_{L1} \cdot (D_{M1} + D_{\text{S1}})}{2} = \dfrac{V_{\text{in1}} \cdot D_{\text{S1}} \cdot T_{\text{s}} \cdot (D_{M1} + D_{\text{S1}})}{2L_1} \\ I_{L2} = \dfrac{\Delta i_{L2} \cdot (D_{M2} + D_{\text{S2}})}{2} = \dfrac{V_{\text{in2}} \cdot D_{\text{S2}} \cdot T_{\text{s}} \cdot (D_{M2} + D_{\text{S2}})}{2L_2} \end{cases} \tag{26}$$

$$\Delta i_{L1} \cdot D_{M1} = \Delta i_{L2} \cdot D_{M2} \tag{27}$$

$$V_{\text{in1}} \cdot I_{L1} + V_{\text{in2}} \cdot I_{L2} = \frac{V_{\text{o}}^2}{R} \tag{28}$$

Substituting (27) and (28) into (26), (29) and (30) can be deduced, respectively,

$$\frac{V_{\text{in1}} \cdot D_{\text{S1}} \cdot D_{M1}}{L_1} = \frac{V_{\text{in2}} \cdot D_{\text{S2}} \cdot D_{M2}}{L_2} \tag{29}$$

$$\frac{V_{\text{in1}}^2 \cdot D_{\text{S1}} \cdot T_{\text{s}} \cdot (D_{M1} + D_{\text{S1}})}{2L_1} + \frac{V_{\text{in2}}^2 \cdot D_{\text{S2}} \cdot T_{\text{s}} \cdot (D_{M2} + D_{\text{S2}})}{2L_2} = \frac{V_{\text{o}}^2}{R} \tag{30}$$

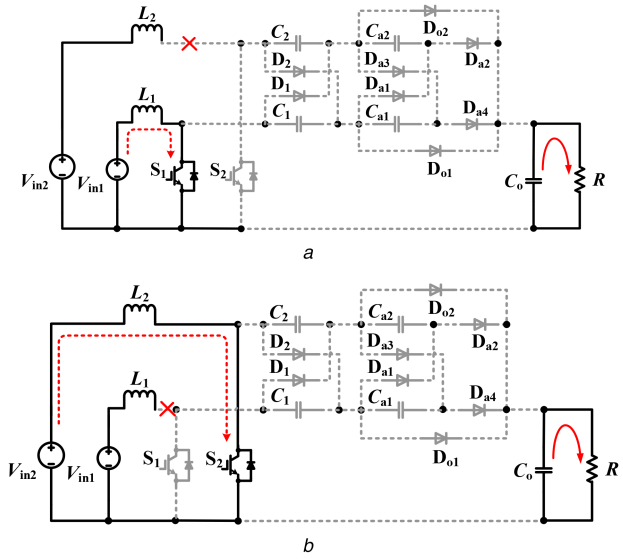

Fig. 13 *Two additional modes when the converter is operating in DCM* ***(a)*** Mode 4 [t_4–t_5], ***(b)*** Mode 8 [t_8–t_9]

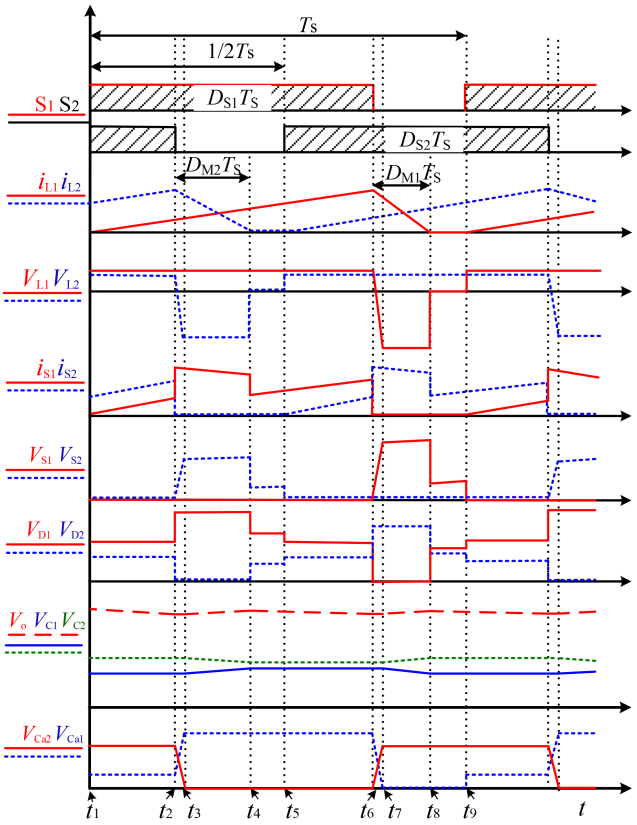

Fig. 14 *Key waveforms of the proposed converter working in DCM during one switch period*

Apparently, by using (25), (29), and (30), the output voltage of the proposed converter in DCM can be obtained as follows: (see (31))

$$V_{\text{o}} = \frac{(V_{\text{in1}} + V_{\text{in2}}) + \sqrt{(V_{\text{in1}} + V_{\text{in2}})^2 + (2(V_{\text{in1}}^2 D_{\text{S1}}^2 T_{\text{S}} R L_2 + V_{\text{in2}}^2 D_{\text{S2}}^2 T_{\text{S}} R L_1)/L_1 L_2)}}{2} \tag{31}$$